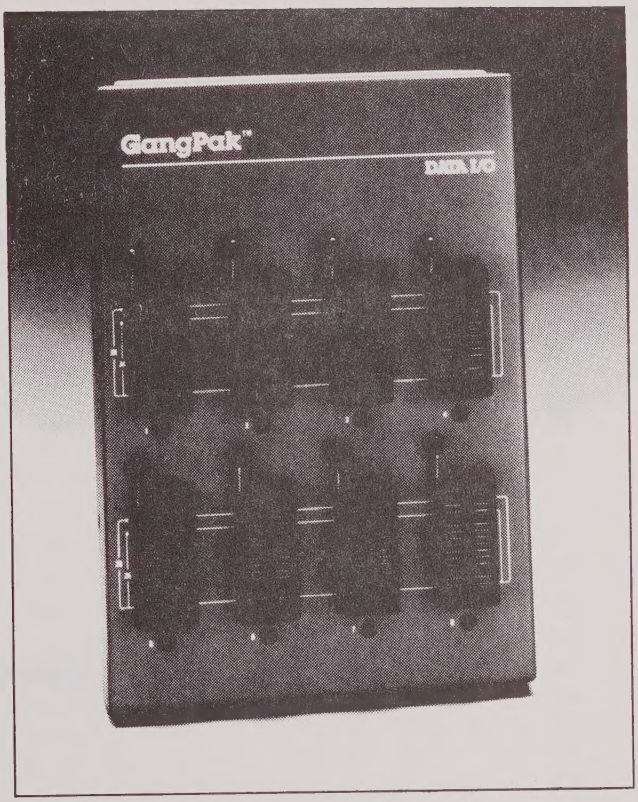
DATA I/O



GangPak™

981-0004-001 REV A JANUARY 85

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Data I/O reserves the right to make changes to this document without notice at any time.

NOTE

Before using the GangPak™, read section 1.3 for programmer mainframe compatibility information.

In general, if a programming voltage is applied to a device which has been inserted backward, catastrophic failure will occur. To minimize part loss, GangPak™ uses circuitry and software to test for backward devices. Devices that are detected are flagged by lit LEDs and error indicators. Due to the electrical characteristics of some parts, backward device testing may damage a percentage of the parts installed backward. Such damage will be identified in further programming operations. Every effort should be made by the operator to ensure that all devices are installed correctly.

Applies to: Engineering Part Number 950-0077-005
Text Reference Number 090-0224

TABLE OF CONTENTS

SECTION 1. INTRODUCTION

1.1 OVERVIEW 1-1
1.2 THEORY OF OPERATION 1-2
1.2.1 Software-Controlled Device Selection 1-2
1.2.2 Electronic Device Identification 1-2
1.2.3 Multi-Image Programming 1-2
1.3 PROGRAMMER COMPATIBILITY 1-5
1.4 APPLICATIONS 1-6
1.5 SPECIFICATIONS 1-6
1.6 FIELD APPLICATIONS SUPPORT 1-6
1.7 WARRANTY 1-6
1.8 SERVICE 1-6
1.9 ORDERING 1-6

SECTION 2. INSTALLATION

2.1 INSPECTION 2-1
2.2 GANGPAK™ INSTALLATION 2-1
2.3 GANGPAK™ REMOVAL 2-2
2.4 REPACKING FOR SHIPMENT 2-2

SECTION 3. OPERATION

3.1 OVERVIEW 3-1
3.2 POWER UP 3-2
3.3 POWER DOWN 3-2
3.4 BASIC OPERATION 3-2
3.4.1 Family Code and Pinout Code Selection 3-3
3.4.2 Device Insertion 3-3
3.4.3 Device Removal 3-3
3.4.4 Load RAM with Master Device Data 3-4
3.4.5 Program Device with RAM Data 3-5
3.4.6 Verify RAM Data Against Master Device Data 3-5
3.5 SELECT CODES 3-6
3.5.1 Clear Silicon Signature ID Check (BC) 3-6
3.5.2 Set Silicon Signature ID Check (BD) 3-6
3.5.3 Examine Family Code and Pinout Code (CC) 3-6
3.5.4 Display a Device's Identifier Array (CD) 3-7
3.5.5 EEPROM Erase Routine (EY 3-7
3.5.6 Select Set Size (E1) 3-7
3.5.7 Select Word Size (E2) 3-8
3.5.8 Display Check Sum of the Desired Device (E3) 3-8
3.5.9 Display GangPak™ Configuration Number (EF) 3-9

SECTION 4. MAINTENANCE/TROUBLESHOOTING/CALIBRATION

4.1 OVERVIEW 4-1
4.2 MAINTENANCE 4-1
4.2.1 GangPak™ Disassembly 4-1
4.2.2 Cleaning 4-2
4.2.3 Inspection 4-2
4.2.4 GangPak™ Assembly 4-2
4.3 TROUBLESHOOTING 4-2
4.3.1 No System Operation 4-2
4.3.2 Poor Yields 4-3
4.3.3 GangPak™ Failure 4-3
4.4 CALIBRATION 4-3
4.4.1 DC Calibration 4-5
4.4.2 Optional Verify-Voltage Checks 4-7
4.4.3 Waveform Observation 4-7
4.4.4 Detailed Explanation of the Timing Diagrams 4-8

SECTION 5. CIRCUIT DESCRIPTION

5.1 OVERVIEW 5-1
5.2 GENERAL ARCHITECTURE/COMPONENT LAYOUT 5-1
5.2.1 Digital Card 5-2
5.2.2 Socket Card 5-2
5.2.3 Waveform Card 5-4

APPENDIX A

FAMILY CODES AND PINOUT CODES A-2
ERROR CODES A-4
MEASUREMENT CHART A-6
TIMING DIAGRAMS A-14
SCHEMATICS A-71
30-701-1822 Digital Card
30-701-0110 Waveform Generator
30-701-0109 Socket Board
30-702-1999 Motherboard

LIST OF FIGURES

1-1 Partitioning Data into PROM-Sized Blocks 1-2
1-2 Example of Set Programming Operation for Set Size of Three 1-3
1-3 32-Bit-Wide Word System 1-3
1-4 Word Programming 1-4
1-5 Example of Set and Word Size Combination Programming of 16K Words 1-4
1-6 Example of a "Modification Status" Sticker 1-5
2-1 GangPak™ Installation 2-1
3-1 Typical 29A Programmer Operation 3-1
3-2 Programmer Power Switch Location 3-2
3-3 GangPak™ Sockets and Device Installation 3-3
4-1 GangPak™ Disassembly 4-1
4-2 Socketboard Interconnect Cable Disconnect 4-1
4-3 Circuit Board Removal 4-2
4-4 Calibration Setup 4-6
4-5 Pin Numbers of Device Sockets 4-7
4-6 Adjustment Locations 4-7
4-7 Scope Trigger Test Point 4-8
4-8 Pin Names by Pinout Code Numbers 4-9
4-9 Sample Timing Diagram 4-10
5-1 Principal Components 5-1
5-2 Block Diagram, GangPak™ Electronics 5-1
5-3 Block Diagram, Digital Card (701-1822) 5-2
5-4 Block Diagram, Socket Board (701-0109) 5-3
5-5 Block Diagram, Waveform Generator (701-0110) 5-4

LIST OF TABLES

1-1 Using the GangPak™ 1-1
1-2 Programmer Compatibility 1-5
1-3 Programmer RAM-Expansion Kits 1-6
4-1 GangPak™ Troubleshooting Chart 4-4
4-2 Key Sequence to Access the Calibration Mode 4-6
A-1 Family Codes and Pinout Codes A-2
A-2 Error Codes A-4
A-3 Measurement Chart A-6

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SECTION 1
INTRODUCTION

1.1 OVERVIEW

Data I/O's GangPak™ gang programming module reliably programs over 40 industry standard 24- and 28-pin EPROMS and EEPROMs. With "set programming" the GangPak™ can download data from a microprocessor development system and partition it into blocks, with up to eight devices per set. Data for wide-word systems (up to 64 bits) can be interwoven within the downloaded data. The GangPak™ also programs up to eight devices with identical data at one time.

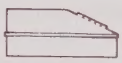
Values for programming variables, including pinouts, voltage levels and timing, are stored in the GangPak™ firmware tables. When you choose the family and pinout codes for a particular device, the programmer uses information in these tables to assemble a specialized programming routine in scratch RAM. This method allows high-speed operation with minimum firmware. The GangPak™ is designed to adapt to the programming requirements of future devices with simple software upgrades.

This manual describes the components and operation of the GangPak™. Subjects addressed in this manual and the corresponding sections are listed in table 1-1. Use this list as a quick-reference point of the major sections in this manual.

Throughout this manual, the entries that you are to make from either the programmer or the terminal are indicated by the entry enclosed in a key symbol. For example,

indicates you should press the "COPY" key on the programmer keyboard. In addition, the symbols shown below are used to indicate modes of operation.

Terminal Mode



Programmer Front Panel Mode

Table 1-1. Using the GangPak™ Manual

Subject	Section
Theory of operation	1.2
Installation procedures for GangPak™	2.0
Basic operation instructions for GangPak™	3.0
Exact key sequences for operating GangPak™ with the 29A Universal Programmer (Refer to your programmer manual for System 19 and 100A key sequences.)	3.0
Maintenance/Calibration/Troubleshooting	4.0
Circuit descriptions	5.0
Block diagrams	5.0
Schematics	5.0
Family codes and pinout codes	Appendix A
Data I/O service centers	Back of manual
Warranty information	Back of manual

1.2 THEORY OF OPERATION

The GangPak™ can be used in 29A, 100A or System 19 programmers of any configuration (see section 1.3 for the required firmware revision levels). There are two methods of programming available with the GangPak™: gang programming and multi-image programming (wide-word programming or set programming described in sub-section 1.2.3). In both cases, when using a master device or a master set as the data source for programming, you must first instruct the programmer to copy the device data into programmer RAM, then enter the family code and pinout code (as described in subsections 1.2.1 and 3.4). When devices with electronic identification are used, the GangPak™ can automatically select the proper family code and pinout code for you (see subsections 1.2. and 3.5 for details).

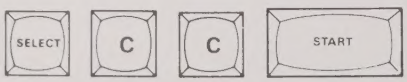
1.2.1 Software-Controlled Device Selection

Your GangPak™ has been designed to program 24- and 28-pin PROMs in the same 28-pin sockets without adapters, configurators or characterizers. This is made possible through the use of software-controlled hardware. The operator simply enters in a four-digit code (a two-digit family code number and a two-digit pinout code number) and the GangPak™ automatically configures its hardware for that device.

Each device is assigned a family code and a pinout code. Devices and their corresponding family codes and pinout codes can be found in table A-1 in appendix A. The family portion of the code specifies information pertaining to the characteristics and requirements of a device. This includes such things as the programming algorithm type and program pulse width; details on the information specified by the various family codes can be found on the measurement chart in section 4. The pinout portion of the code specifies information on the physical layout of a device such as the location of the address pins and the location of the control pins and their active states; details on the information specified by the various pinouts can be found on the pinout chart in section 4.

1.2.2 Electronic Device Identification

The GangPak™ can be instructed to automatically configure itself to program PROMs that have been encoded with an electronic identifier by the manufacturer. You can do this by selecting "FF FF" when prompted for the family and pinout codes by the programmer. When you do this, the GangPak™ will read the electronic identifier encoded into the device and select the correct family code and pinout code for you. To see what codes were automatically chosen, press



then the programmer will display the codes. This select function will only work after you have initiated a device-related operation (such as a Load operation). If you try to select this function before you have initiated a device-related operation, the programmer will display 0000 **.

When using this feature, be sure that the parts have the manufacturer's electronic identifier and that all the devices program the same way. The GangPak™ will automatically check to ensure that this has been done.

1.2.3 Multi-Image Programming

Your GangPak™ can simultaneously program two to eight PROMs with completely different data patterns. This feature eliminates the need for separate down-load and programming operations, saving time and eliminating confusion. There are two ways in which the GangPak™ makes this feature available: selectable modes called set programming and word programming (see section 3.5 for operational information). Both modes take advantage of common data presentation schemes. These modes (set programming and word programming), as well as using these modes together, are described in this subsection.

Set Programming

It is common for the length of a program to exceed the capacity of a single PROM (as shown in ① of figure 1-1). Loading the program data into PROMs, therefore, requires that the data be partitioned into appropriately sized blocks to be programmed into multiple PROMs, as shown in ② on figure 1-1; the size of each block would be determined by the capacity of the PROM being used. Once partitioned, each block of data would then be programmed into an individual PROM, as shown in ③ on figure 1-1. The programmed PROMs comprise what is referred to as a "set" since, together, they contain the complete range of data (the original program).

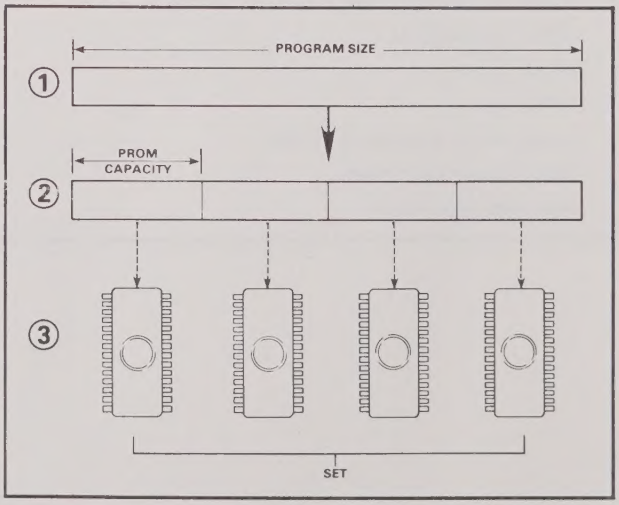


Figure 1-1. Partitioning Data Into PROM-Sized Blocks

The GangPak™ eliminates the need to manually partition these data into blocks and program each partition separately. You simply enter the number of devices in the set and an entire set of PROMs can be created in just one program operation in the time it would otherwise take to program a single device. The number of devices in the set, called set size, can range from one to eight and is selected through the select function (E1, see section 3.5 for details).

For set sizes of less than five, multiple sets of PROMs can be produced simultaneously. The first PROM of the second set is always placed in the next higher socket number following the last PROM of the preceding set. To clarify this, refer to figure 1-2, which illustrates set programming for a set size of three. In this example, the first PROM of the set is shown as "A" and last PROM in the set is shown as "C". Notice that the first PROM of the second set, also shown as A, has been inserted in the next socket after C (the last PROM in the preceding set). Extra sockets forming an incomplete set are to be left unused and are designated as illegal. Thus, if you place devices in these sockets during a device operation, it will generate error message A-9 (illegal insertion).

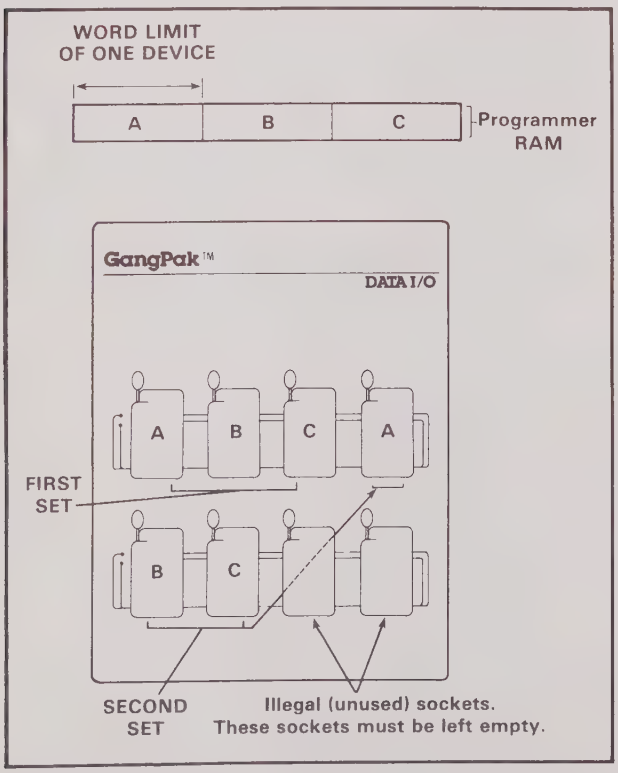


Figure 1-2. Example of Set Programming Operation for Set Size of Three

Word Programming

Most PROMs are organized into 8-bit bytes, each address in the PROM accessing one byte of data. This scheme is fine for byte-wide (8 bits per byte) processors. As the need for greater computing power increased, semiconductor manufacturers have introduced microprocessors with wider data bus structures. Today, wide-word microprocessors with data bus widths of 16 and 32 bits are not uncommon. PROMs, however, have continued for the most part to be organized by 8 bits per byte.

One way to use these PROMs in wide-word systems is to organize several PROMs in such a manner as to allow each address to access several bytes simultaneously. A group of PROMs organized in this fashion can be considered as one virtual PROM organized into 16- or 32-bit words, each address accessing one word; figure 1-3 illustrates this scheme for a 32-bit-wide word system.

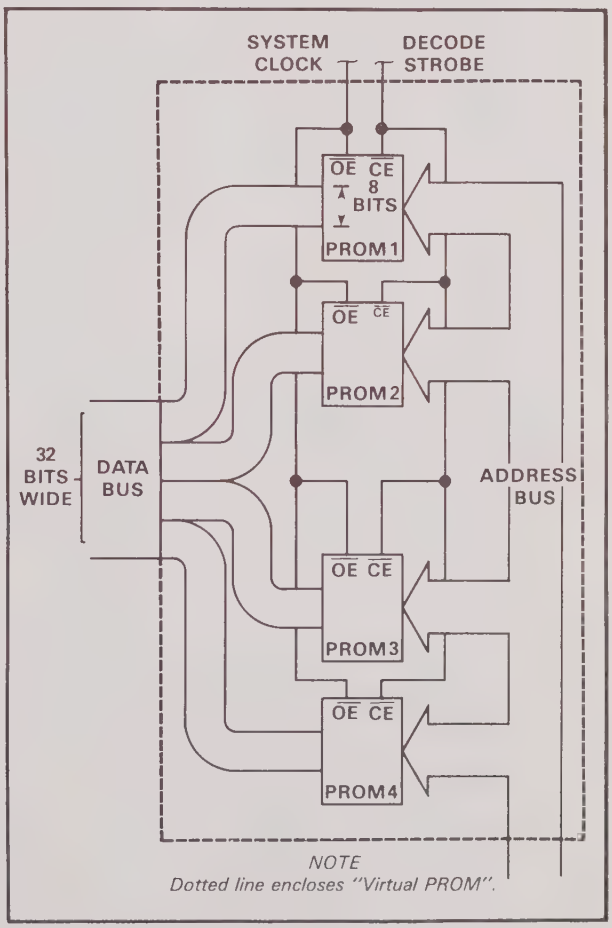


Figure 1-3. 32-Bit-Wide Word System

In this scheme, the address and decode of the individual PROMs are wired in parallel — that is, they are shared in common. Each PROM contributes 8 bits to the 32-bit word. Thus, when address Ø is accessed, for instance, PROM 1 would output the high-order byte of the word, PROM 2 would output the upper middle, PROM 3 the lower middle, and PROM 4 would output the low order. PROM 1 could be considered the high-order PROM, since it will contain only the high-order portion of the word at all its addresses, and similarly for the other three PROMs.

Data for this scheme would typically be assembled by a development system in the form of consecutive words: each word made up of a high-, upper-middle, lower-middle, and low-order bytes. Data in this format could be downloaded directly to the programmer's RAM to be programmed into PROMs by the GangPak™. By selecting the proper word size, the GangPak™ would then automatically distribute the appropriate data to each PROM. Thus, time-consuming, tricky and messy data manipulations are totally unnecessary with your GangPak™ for data arranged in the form of words up to 64 bits wide. These word size selections are accessed through a select code (described in section 3.5).

Figure 1-4 illustrates how the data would be programmed into the PROMs using the GangPak™. As can be seen in this figure, the PROMs in sockets 1 and 5 would contain the byte at BEGIN RAM ADDRESS and every subsequent fourth byte, PROMs 2 and 6 would contain the byte at the BEGIN RAM ADDRESS +1, and every fourth byte from there, etc. Thus, in one program operation, two sets of PROMs could be created.

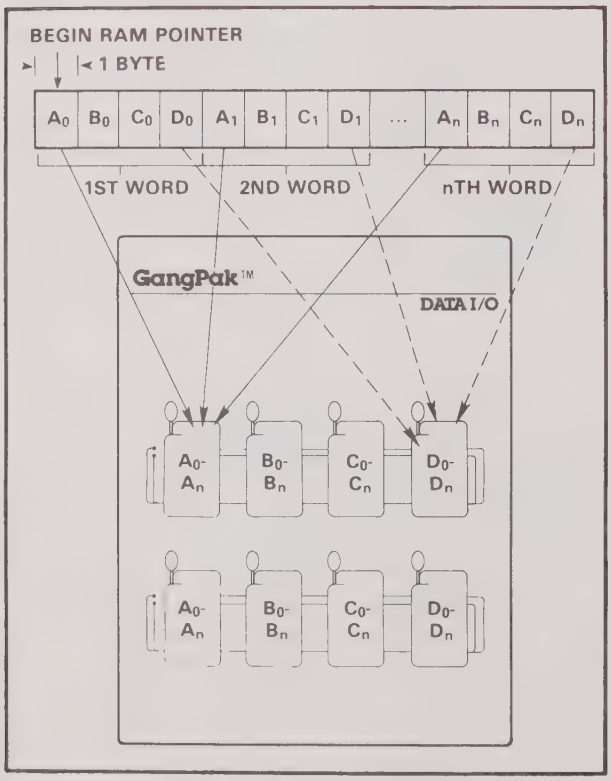


Figure 1-4. Word Programming

Set and Word Size Combinations

The GangPak™ also enables you to select set and word size combinations. This mode is useful when one needs to program a large block of data that is arranged by words. For example, if one were to download a file of 16K words, each word being 2 bytes wide, and wanted to program them into a set of 4K x 8 bit PROMs, he would select a set size of 4 and a word size of 16. When selecting set and word size combinations, the rule of thumb is: SET SIZE X WORD SIZE $\leq$ 64. Using this rule of thumb ensures that the GangPak™ has enough sockets to accommodate the operation. Figure 1-5 shows how the GangPak™ will distribute the data.

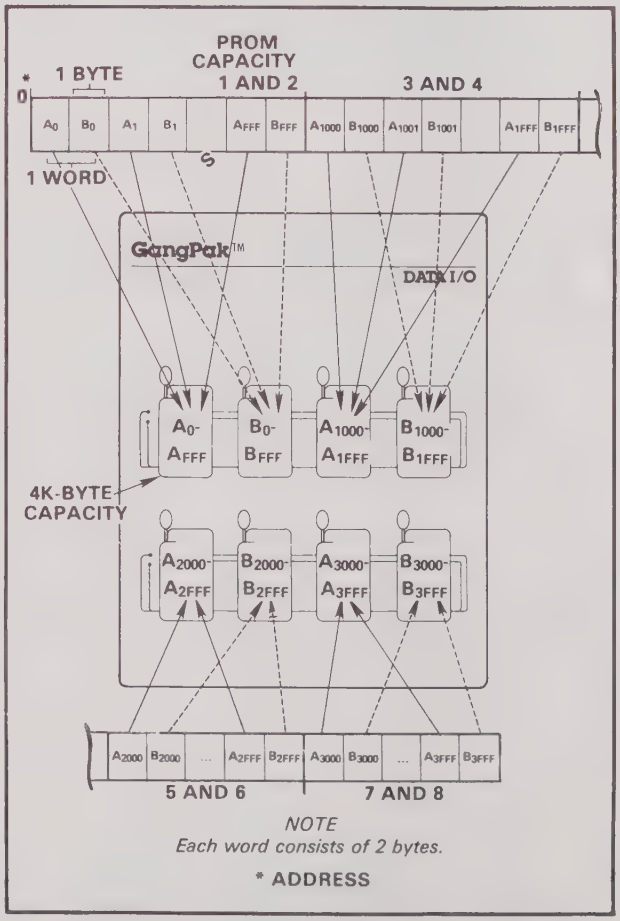


Figure 1-5. Example of Set and Word Combination Programming of 16K Words

1.3 PROGRAMMER COMPATIBILITY

To be compatible with the GangPak™, your programmer may require a hardware and/or firmware update, depending on the model, configuration, and age. The information that follows will help you determine whether your programmer requires updating. If you find that your programmer does require updating, contact your nearest Data I/O Service Center.

- System 17 — The System 17 must be converted into a System 19 with the latest firmware installed and latest hardware modifications.

NOTE
Devices that are 512 kbits or greater cannot be programmed in a System 17.

- System 19 — Check to determine whether your System19 contains a 702-1520 or 702-1980 controller board by performing the following steps:

1. Remove the programming pak (section 2.3).
2. Remove the metal shield on the programmer (if any, see figure 2-1).
3. Count the number of EPROM firmware sockets located just behind the pak interface connector. If there are four sockets, it is a 702-1520 board. If there are eight sockets, it is a 702-1980 board.

If your System 19 contains a 702-1520 controller board, check the modification status sticker (figure 1-6) on the bottom of the programmer. If the sticker is not there or if only "1" is marked off, your System 19 requires hardware and firmware updating; contact the nearest Data I/O Service Center. If "2" is marked, your System 19 is compatible with the GangPak™.

MODIFICATION STATUS

1	2	3	4	5	6
0	0	0	0	0	0

Figure 1-6. Example of a "Modification Status" Sticker

If your System 19 contains a 702-1980 controller board, it may require a firmware update. To display the configuration number of the firmware in your programmer, key in "SELECT-B2-START." If the configuration number displayed is either "3599" or "CC8B", your firmware needs updating.

NOTE
Devices that are 512 kbits or greater cannot be programmed in a System 19.

- 29A Universal Programmer — To be compatible with the GangPak™, the 29A programmers must have Rev C or later firmware. To determine the configuration of the firmware in your 29A, key in "SELECT-B2-START" and observe the display. Refer to table 1-2 to determine if your firmware needs to be updated.

NOTE
Rev D or later firmware must be installed in the 29A to program 512 kbit devices.

- 29B Universal Programmer — Does not require any revisions to be compatible with the GangPak™.

Table 1-2. Programmer Compatibility

Model	Rev	Configuration Number
29A	A B	1ECA 20A4
29A (with computer remote control)	A B	BB41 C00B
100A	A B C D	917F 9405 9DEE 9BED

- 100A Production Programmer — To be compatible with the GangPak™, the 100A programmers must have Rev E or later firmware. To determine the configuration of the firmware in your 100A, key in "SELECT-1Ø" and observe the display. If the hex number display matches one listed in table 1-2, your firmware needs to be updated.

  Devices that require more RAM than is available in the System 100A cannot be programmed.

  To fully utilize the set programming feature of the GangPak™, the RAM expansions shown in table 1-3 are available.

Table 1-3. Programmer RAM-Expansion Kits

MODEL	STANDARD RAM	MOTHERBOARD	EXPANDED RAM	RAM-EXPANSION KIT
29A	8K x 8	1980	16K x 8 64K x 8	951-0100-001
100A	4K x 8	1980	8K x 8 16K x 8	951-0100-002
System 19	4K x 8	1980	8K x 8 16K x 8	951-0100-002 951-0100-001
		1520	8K x 8 16K x 8	950-1533-1 950-1533-2

1.4 APPLICATIONS

Table A-1 in appendix A lists all the devices that could be programmed with the GangPak™ at the time this manual was published. In many cases when a new device with industry-standard pinout is introduced within a manufacturer's family, the GangPak™ WILL NOT require a revision to program it. For some new applications, such as to accommodate a new device family, a firmware update of the GangPak™ may be required. The revision number is stamped after the part number (950-0077) along the underside of the top edge of the GangPak™ socket assembly.

1.5 SPECIFICATIONS

The GangPak™ receives its power from the programmer mainframe. Programming waveforms are generated from raw programmer supplies using regulators controlled by the programmer's microprocessor. The controlling firmware is located on a circuit card within the GangPak™.

The physical and environmental specifications are:

- Altitude: Sea level to 3 km (10,000 ft)
- Dimensions: 6¾ x 9½ x 4½ in.
- Humidity (operating): 90% maximum (noncondensing)
- Humidity (storage): 95% maximum (noncondensing)
- Temperature (operating): 0 to 40°C (32 to 104°F)
- Temperature (storage): −40 to 55°C (−40 to 131°F)
- Weight: 1.48 kg (3 lb, 4 oz)

1.6 FIELD APPLICATIONS SUPPORT

Data I/O has Field Applications Engineers (FAEs) throughout the world. They can provide additional information about interfacing Data I/O products with other equipment and answer questions about equipment. FAEs are located within the United States at the addresses listed in the back of this manual. For international applications support, contact your nearest Data I/O representative.

1.7 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period of one year begins when you receive the equipment. The warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O Service Center.

1.8 SERVICE

Data I/O maintains Service Centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. In addition to repairs, all Data I/O products can be calibrated at Service Centers. A list of all Data I/O Service Centers is located in the back of this manual.

1.9 ORDERING

To order equipment, contact your Data I/O sales representative. Orders must contain the following information:

- Description of the equipment (see the latest Data I/O price list or contact your sales representative for equipment and part numbers)
- Quantity of each item ordered
- Shipping and billing address of firm, including ZIP code
- Name of person ordering equipment
- Purchase order number
- Desired method of shipment

SECTION 2
INSTALLATION

2.1 INSPECTION

The GangPak™ was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should, therefore, arrive free of any defects, without marks or scratches, and in perfect operating condition. Carefully inspect the instrument for any damage that may have occurred in transit; if you note any damage, file a claim with the carrier and notify Data I/O.

NOTE

Voltage transients can cause device damage. Be sure that all sockets are empty when:

- *Switching power on or off*

or

- *Installing or removing the GangPak™*

2.2 GANGPAK™ INSTALLATION

The GangPak™ may be installed and removed with the programmer's power on; this feature allows you to retain data in RAM during module changes. If the programmer power is turned on before the GangPak™ is installed, you will hear a "beep" until the GangPak™ is installed.

To install the GangPak™, do the following:

1. Slide the GangPak™ into the opening in the programmer (figure 2-1).
2. Tilt the GangPak™ up and gently push it back to hook the flange of the GangPak™ over the back edge of the programmer opening (figure 2-1a).
3. Lower the GangPak™ into position as shown in figure 2-1b.
4. Press gently on the front edge of the GangPak™ to ensure a good connection (figure 2-1c).

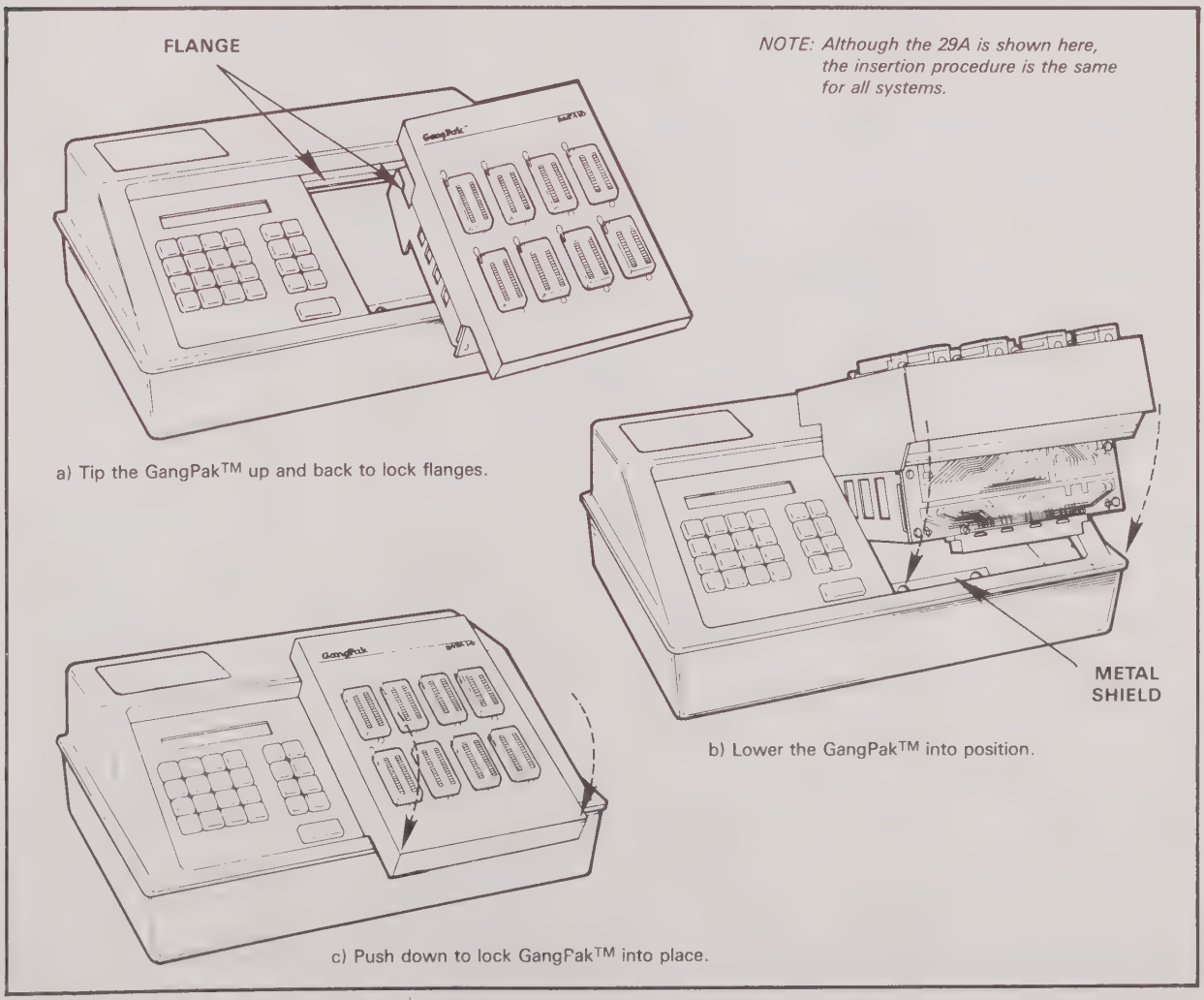

FLANGE
NOTE: Although the 29A is shown here, the insertion procedure is the same for all systems.
a) Tip the GangPak™ up and back to lock flanges.
METAL SHIELD
b) Lower the GangPak™ into position.
c) Push down to lock GangPak™ into place.

Figure 2-1. GangPak™ Installation

2.3 GANGPAK™ REMOVAL

1. Check to make sure the programmer is not in the middle of an operation. If it is, wait until the operation is complete (the action symbol on the display disappears).
2. Check to make sure a device is not in a socket. If one is in a socket, remove it as described in section 3.7.
3. Tilt the GangPak™ up and gently remove it from the programmer.

2.4 REPACKING FOR SHIPMENT

If the GangPak™ is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number, revision level, and name. If the original shipping container is to be used, place the GangPak™ in the container with the appropriate packing material and seal the container with strong tape. If another container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

SECTION 3

OPERATION

3.1 OVERVIEW

The GangPak™ can be used in 29A, 100A or System 19 programmers of any configuration; see section 1.2 for firmware revision levels required. There are three methods of programming available with the GangPak™: gang programming, set programming and word programming.

The typical gang programming operation with a 29A programmer and a GangPak™ is illustrated in figure 3-1. As can be seen from this figure, the GangPak™ can obtain data from three sources (a master device(s), a serial port, or the keyboard); because the serial port and keyboard operation are unique for each type of programmer, you will be referred to your System 19 or 100A programmer manual for details on how to program using these mainframes.

The procedures to perform basic operations with your GangPak™ and the 29A are described in this section.

Wherever possible, key sequences have been included to use your GangPak™ with a 29A Universal Programmer with Rev D firmware (read section 1.3 carefully to determine your programmer's firmware revision level). Refer to your programmer manual for key sequences for the 19 and 100A programmers.

Throughout this manual, the entries that you are to make from either the programmer or the terminal are indicated by the entry enclosed in a key symbol. For example,

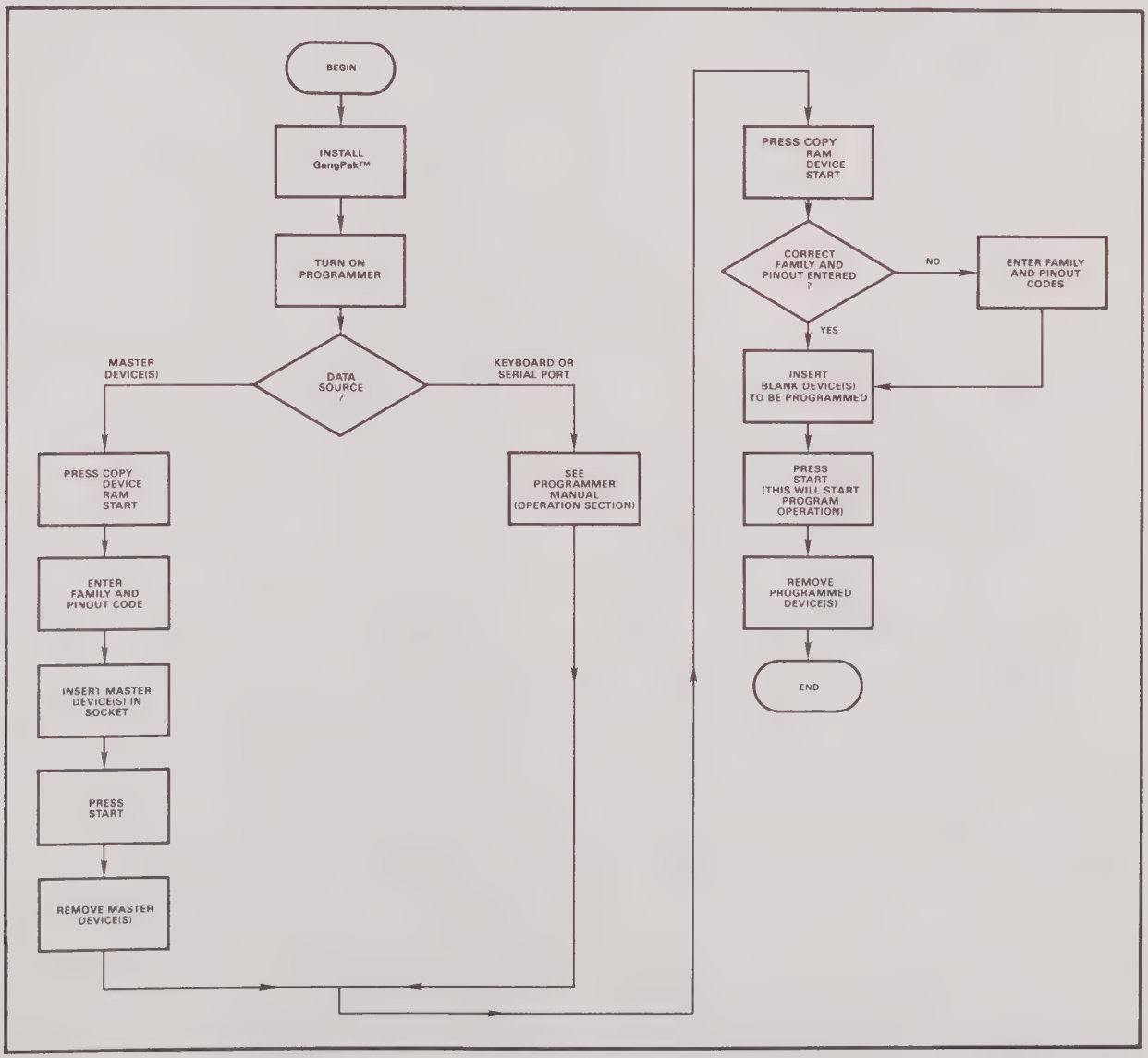
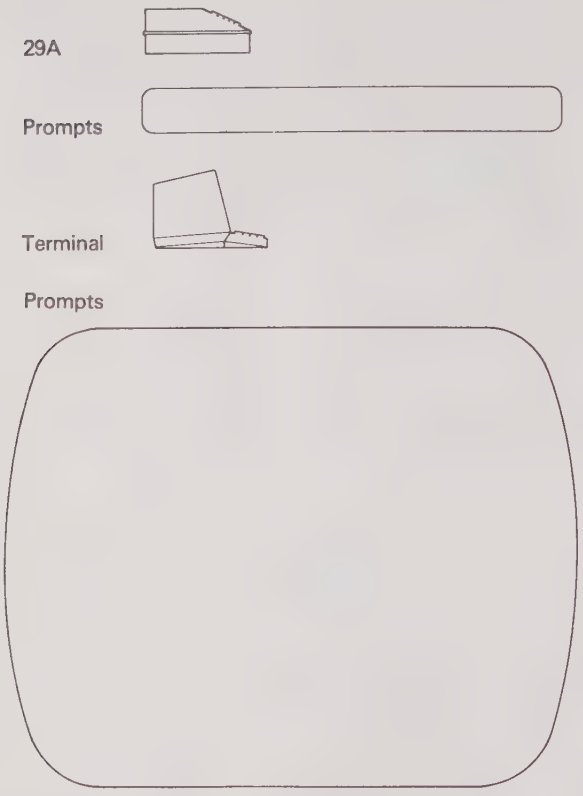


Figure 3-1. Typical 29A Programmer Operation

indicates the "ESC" (escape) key on the terminal keyboard should be pressed. In addition, the symbols shown below are used to indicate modes of operation and prompts.



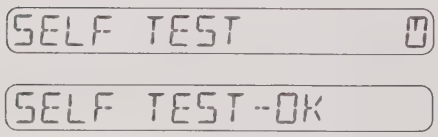
3.2 POWER UP

If the GangPak™ is not installed in the programmer when power is turned on, you will hear a "beep" until the GangPak™ is properly installed.

When power is fully applied, the programmer will perform the self-test routine. When the self-test routine is complete, the programmer will display its ready message.

NOTE

The line in the action Symbol (⊡) rotates 360 degrees several times as the programmer performs the self test. When the self test is complete, the programmer displays



To turn the programmer on:

1. Check to make sure the sockets are empty. If a device is in a socket, lift up the lever (on the upper left of the socket; see subsection 3.4.3), then gently lift the device out of the socket.
2. Plug one end of the AC power cord into a power outlet and the other end into the power cord connector on the back of the programmer.
3. Lift the power switch up to the "ON" position (see figure 3-2).

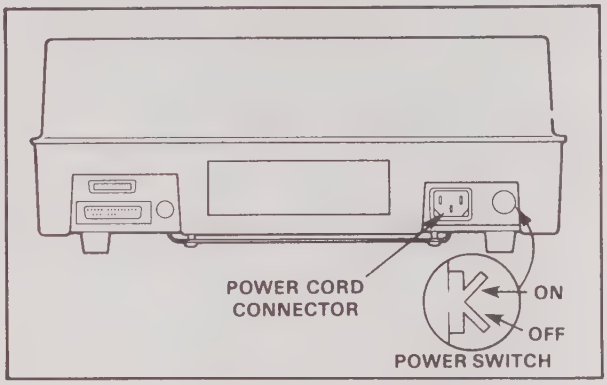


Figure 3-2. Programmer Power Switch Location

3.3 POWER DOWN

CAUTION

Do not turn the power off while the programmer is doing an operation or when a device is in a socket; voltage transients may damage the device.

To turn the programmer power off, do the following procedure:

1. Check the action symbol on the programmer display to make sure that the programmer is not in an operation process. If the action symbol has not stopped, wait until the operation is complete and the action symbol has stopped turning.
2. Check to make sure the sockets are empty. If a device is in a socket, remove it as described in section 3.4.3.
3. Push the power switch down to the "OFF" position (figure 3-2).

3.4 BASIC OPERATION

The GangPak™ has eight sockets that can be used to program from one to eight devices at the same time. All data transfer or verification operations occur between the programmer's internal RAM and the device(s) or between the RAM and serial port in your programmer. Because the operating procedure to transfer data via a serial port varies among programmers, this manual describes only data transfer using the 29A. For other programmers, refer to the specific operation manual.

The basic data transfer operations that can be accomplished with the GangPak™ and 29A Universal Programmer are listed below and described in the following subsections:

- Load RAM with data from a master device or master set (described in section 3.4.4).
- Load RAM with data from the serial port (described in your programmer manual).

- Program groups of devices with the same RAM data (described in section 3.4.6).
- Program sets of devices with RAM data (described in section 3.5.3).
- Verify RAM data against the device data (described in section 3.4.6).

3.4.1 Family Code and Pinout Code Selection

Any device that can be programmed with the GangPak™ is specified by a unique combination of a two-digit family code and a two-digit pinout code; see table A-1, appendix A of this manual to find the correct family code and pinout code for the device you are programming. Once the codes are entered for a particular device, the GangPak™ remains set up for any operation with that device until you enter new codes. If invalid family codes and pinout codes are entered, a beep will sound and the operation will be stopped. In the 29A terminal mode, the programmer will display:

```
COMMAND ERROR 17
```

and the operation will be stopped.

To select the family and pinout codes:

1. Locate the manufacturer and part number stamped on the device.
2. Turn to the family and pinout code table (table A-1 in appendix A) and find the manufacturer's name.
3. See the column entitled "Device Part Number" and find the number corresponding to the number on the device.
4. See the columns labeled "Family Code" and "Pinout Code" to find the code numbers corresponding to the device number for the manufacturer of the device.
5. Enter the family code and pinout code you selected from this table when prompted by the programmer or terminal.

3.4.2 Device Insertion

Once you have entered the appropriate family and pinout codes, the GangPak™ is ready to accept devices.

A good electrical connection between a device and its socket is essential. To ensure a good connection:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift the lever on the upper-left side of the socket; see figure 3-3. (The lever will stay in the upright position.)
3. Gently set the device in the socket.

NOTE:

For 28-pin devices, make sure pin 1 of the device is aligned with pin 1 of the socket (upper left corner); see figure 3-3.

For 24-pin devices, make sure pin 1 of the device is aligned with the dot on the 24-pin line of the socket (see figure 3-3) and pin 12 is aligned with the bottom left corner of the socket.

In general, if a programming voltage is applied to a device which has been inserted backwards catastrophic failure will occur. To minimize part loss, GangPak™ uses circuitry and software to test for backward devices. Devices that are detected are flagged by lit LEDs and error indicators.

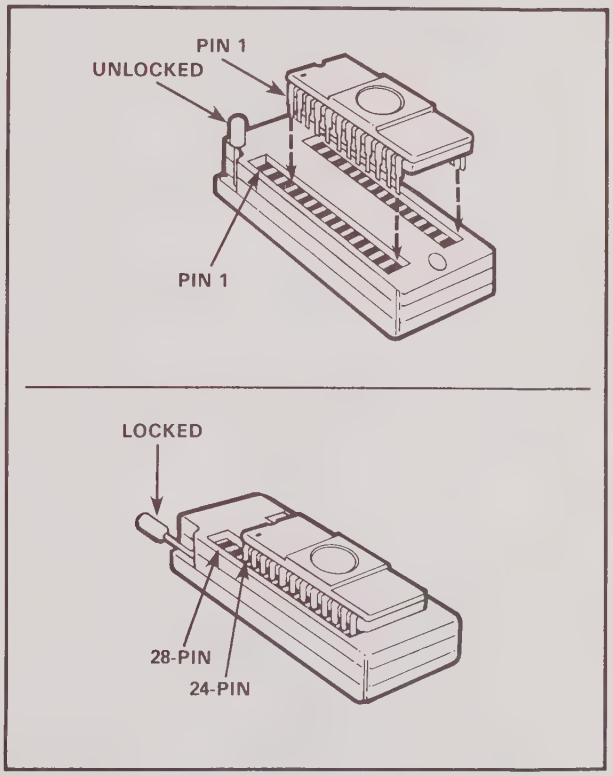


Figure 3-3. GangPak™ Sockets and Device Installation

4. Push the lever down to lock the device in the socket.

3.4.3 Device Removal

To remove a device:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift the lever on the left side of the socket (see figure 3-3). The lever will remain in the upright position.

3.4.4 Load RAM with Master Device Data

To load the 29A RAM with data from a master device with control from programmer front panel, follow the steps given below. A set of master devices of up to eight can be loaded at one time. After the load operation, the set size in effect is automatically set to the number of devices inserted. The set of devices must be installed starting at socket 1 with no gaps of unused sockets between devices in the set. Data are arranged in RAM the way the devices are positioned in the sockets. The data from the device in socket No. 1 are loaded into the lowest block of RAM.

1.

29A Displays

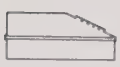
2.

to select the source of the data.

29A Displays

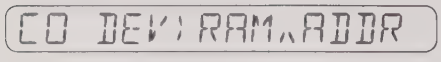
NOTE

ADDR/SIZE pertains to block limit parameters. ADDR is the starting device address. It can be set to any address within the range of the word limit of the device. SIZE is the number of bytes to be considered in the operation and cannot exceed the word limit of one device. If unset, these parameters will default to 0 and the word limit of the device, respectively.

3. 

to select the destination for the data.

29A Displays



NOTE

ADDR is the starting RAM address for the operation.

4.

29A Displays

NOTE

The 29A will display 00 if you have not entered a family code and pinout code or will display the last family code and pinout code you entered.

5. Enter the family code and pinout code (see section 3.4.1).
6. Insert a device(s) into the appropriate socket(s).

7.

29A Displays

NOTE

The amount of time the programmer will require to perform this operation will vary depending on the device size. Lit LED will indicate the devices are being loaded and the action symbol will rotate 360 degrees several times. When the operation is complete, the LED goes off and the action symbol signals the programmer's readiness unless there is an error (see table A-2 in appendix A).

checksum of device data

NOTE

XXXX is the check sum of all the device data. If you have set block limits, the check sum (XXXX) will be calculated only for the device in the first socket. If no devices are detected, the check sum will remain the same as it was before the operation (i.e., the RAM data will be unchanged).

8. Remove the master device(s) from the GangPak™ (see section 3.4.3).

3.4.5 Program Device with RAM Data

When programming a device, the system performs illegal bit tests and blank checks at low V_{CC}.

To program a blank device with the data in the 29A RAM with control from the programmer front panel, follow the steps given below.

NOTE

If changes are desired for set size and/or word size, make changes as needed before proceeding.

1.

to select the destination for the data.

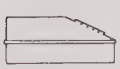
29A Displays

2.

29A Displays

NOTE

ADDR/SIZE pertains to block limit parameters. ADDR is the starting RAM address. It can be set to any address within the range of RAM with which your programmer is equipped. SIZE is the number of bytes to be considered in the operation. If unset, these parameters will default to 0 and the word limit of the device, respectively.

3. 

29A Displays

NOTE

ADDR is the starting device address for the operation.

4.

Family code Pinout code

NOTE

The 29A will display 00 if you have not entered a family code and pinout code or will display the last family code and pinout code you entered.

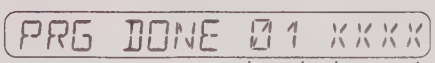
5. Enter the family code and pinout code (see section 3.4.1).
6. Insert a device(s) into the appropriate socket(s).

29A Displays

NOTE

During programming, the LED under the devices will be lit.

When programming and verify are complete, the LED under the socket that has failed is lit. LEDs of empty sockets are also lit. If a device has programmed correctly, the corresponding LED will go off.



sequence number checksum
(increments by 1 for each programming operation)

3.4.6 Verify RAM Data Against Master Device Data

The two-pass verify consists of comparing the device data to RAM data and is performed at two V_{CC} levels; these levels vary according to each manufacturer's requirements.

To verify that data entered in the 29A RAM duplicates the device data, follow the steps listed below.

1.

29A Displays

2.

29A Displays

3.

29A Displays

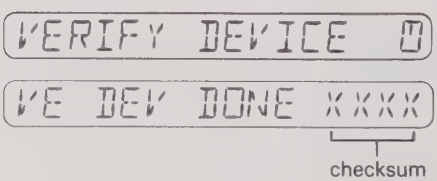
4.

29A Displays

5. Enter the family code and pinout code (see section 3.4.1).
6. Insert the device to be verified into the GangPak™ (see section 3.4.2).

7.

29A Displays



NOTE

LEDs will be lit under all sockets that did not verify or had no part detected in them.

8. Remove the devices from the GangPak™ (see section 3.4.3).

3.5 SELECT CODES

In addition to the three basic source-destination functions (copy, verify and edit) and the select functions described in the Operation section of your programmer manual, the GangPak™ offers nine additional select functions (BC, BD, CC, CD, E0, E1, E2, E3 and EF); these functions are not mandatory for basic operation of the GangPak™. These select functions are described in this section.

3.5.1 Clear Silicon Signature ID Check (BC)

Select function BC disables (clears) an error when the silicon signature ID does not compare with the entered Family Code/Pinout. This select code is used when it is desirable to substitute a different Family Code/Pinout for the one set in the silicon signature. To use the Clear Signature ID select function, follow the steps below.

1.

29A Displays

2.

29A Displays

3. The Silicon Signature ID check device feature is now disabled.

3.5.2 Set Silicon Signature ID Check (BD)

Select function BD enables (sets) an error when the silicon signature ID does not compare with the entered Family Code/Pinout. This select code is used to prevent the accidental destruction of the devices when the wrong Family Code/Pinout is entered. The ID check will be enabled (set) whenever a new Family Code/Pinout is entered. To use the Set Signature ID select function, follow the steps below.

1.

29A Displays

2.

29A Displays

3. The silicon signature ID check device feature is now enabled.

3.5.3 Examine Family Code and Pinout Code (CC)

Select function CC displays the family code and pinout code that the GangPak™ used during the last device-related operation. This select code is useful when "FF FF" has been selected when prompted for the family and pinout codes.

1.

29A Displays

2.

29A Displays

NOTE

XX is the device family code and YY is the pinout code.

3.5.4 Display a Device's Electronic Identifier Array (CD)

Select function CD displays the 16 bytes of the device's electronic identifier. Byte /is the manufacturer's identification; byte 1 is the device's identification. The functions of bytes 2 through 15 are determined by the manufacturer of the device.

To display the electronic identifier encoded in the device, follow the procedure outlined below.

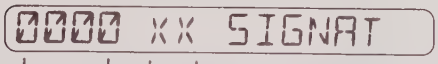
1.

29A Displays

Insert the device into socket No. 1

2.

29A Displays



identifier number (0 to 15)

identifier byte

3.

to increment to the next signature byte

4.

to back up to the previous signature byte

3.5.5 EEPROM Erase Routine (EØ)

Select code EØ allows you to erase (return to its unprogrammed state) an electrically erasable PROM (EEPROM). The correct family code and pinout code must have been entered before this select code is executed.

1.

29A Key Sequence

29A Displays

2.

29A Displays

XX is the device family code and YY is the pinout code.

NOTE

Make sure that the family code and pinout code in the programmer display are correct before continuing. If they are correct, do step 3a. If not correct, do step 3b.

3a. If the family code and pinout code in the programmer display are correct, insert the PROM(s) to be erased into any socket(s). Press START and your PROMs will be erased.

or

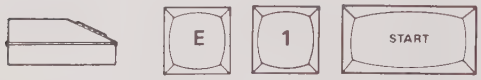
3b. If the family code and pinout code in the programmer display are not correct, exit the select mode by pressing any function key, then enter the correct codes.

3.5.6 Select Set Size (E1)

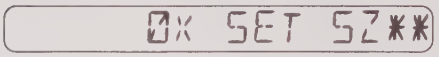
Use this procedure to select the set size when doing set programming. For a description of set programming, refer to subsection 3.5.3.

1.

29A Displays

2. 

29A Displays



NOTE

X is the current set size in effect. The programmer will default to 01 or to the number of devices loaded in the last load operation. To change the defaulted number, just select the correct number.

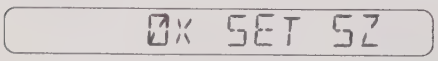
3.

to select the number of parts in a set.

NOTE

X represents the number of parts in a set. This entry can be any number from 1 through 8. If the correct number of parts in the set is displayed, continue with the next step. If it is not the correct number, enter in the correct number.

29A Displays

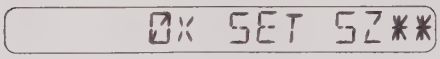


NOTE

When entering set size, remember that the number of parts times the device size must be less than or equal to the programmer RAM size. If the set size exceeds the programmer RAM size, the programmer will accept the entry, but will display ERROR 27 when you attempt a device-related operation.

4.

29A Displays



NOTE

0X is the set size now in effect.

If you do a Load operation for a set of devices, the set size will automatically be set to the number of devices in the set.

3.5.7 Select Word Size (E2)

This procedure enables you to program PROMs for use in wide-word systems (data bus width of greater than 8 bits). To use the word size select function, follow the steps below.

1.

29A Displays

2.

29A Displays

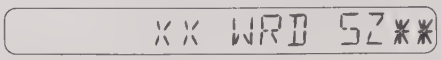
NOTE

XX is the word size currently in effect. The programmer will default to 08.

3. To enter another word size, key in the new number. Possible word sizes are 08, 16, 24, 32, 40, 48, 56, and 64.

4.

29A Displays



3.5.8 Display Check Sum of the Desired Device (E3)

This select code allows one to determine the sum check of a device in any one of the sockets. The correct family and pinout codes must be selected before executing this select code.

1.

29A Displays

2.

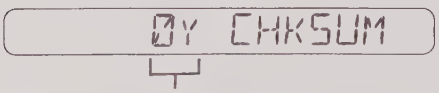
29A Displays

NOTE

01 is the socket number of the device to be summed. The socket number of the device to be summed can be chosen at this time by entering the new socket number (numbers 1 through 8).

3.

29A Displays

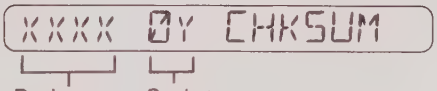


NOTE

0Y is the socket number in which the device whose check sum you are checking is located. The LED of the corresponding socket will light up.

4.

29A Displays



3.5.9 Display GangPak™ Configuration Number (EF)

This command displays the configuration number of the pak firmware. Configuration numbers are used as serial numbers for firmware.

1.

29A Displays

NOTE

XXXX is the configuration number of the firmware.

BLANK

SECTION 4

MAINTENANCE/TROUBLESHOOTING/CALIBRATION

4.1 OVERVIEW

The support material in this section has been provided to help you keep your GangPak™ in good operating condition. General maintenance practices are discussed in section 4.2, while the basic troubleshooting steps are listed in section 4.3. For those GangPak™ users who prefer to do their own calibration, detailed procedures, including measurement charts and timing diagrams, are provided in section 4.4.

4.2 MAINTENANCE

Before the GangPak™ can be cleaned (section 4.2.2) and/or inspected (section 4.2.3), it must be disassembled as described below.

4.2.1 GangPak™ Disassembly

To disassemble the GangPak™, refer to figure 4-1 and the procedure listed below.

1. Remove the GangPak™ from the programmer (see section 2.3 for details).
2. Lay the GangPak™ face down on a flat surface.
3. Unscrew the captive fasteners (figure 4-1a) until they hang loosely; the screws will not separate from their standoffs.
4. Lift the card cage up slightly, then pull it out (as shown in figure 4-1b) to unlock the flanges.
5. Lift the card cage up until you can see the socketboard interconnect cable and its connector (figure 4-2).

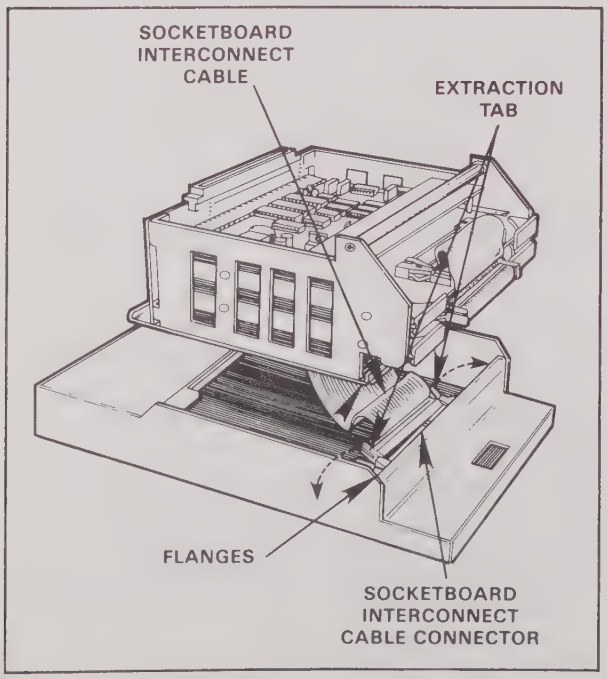
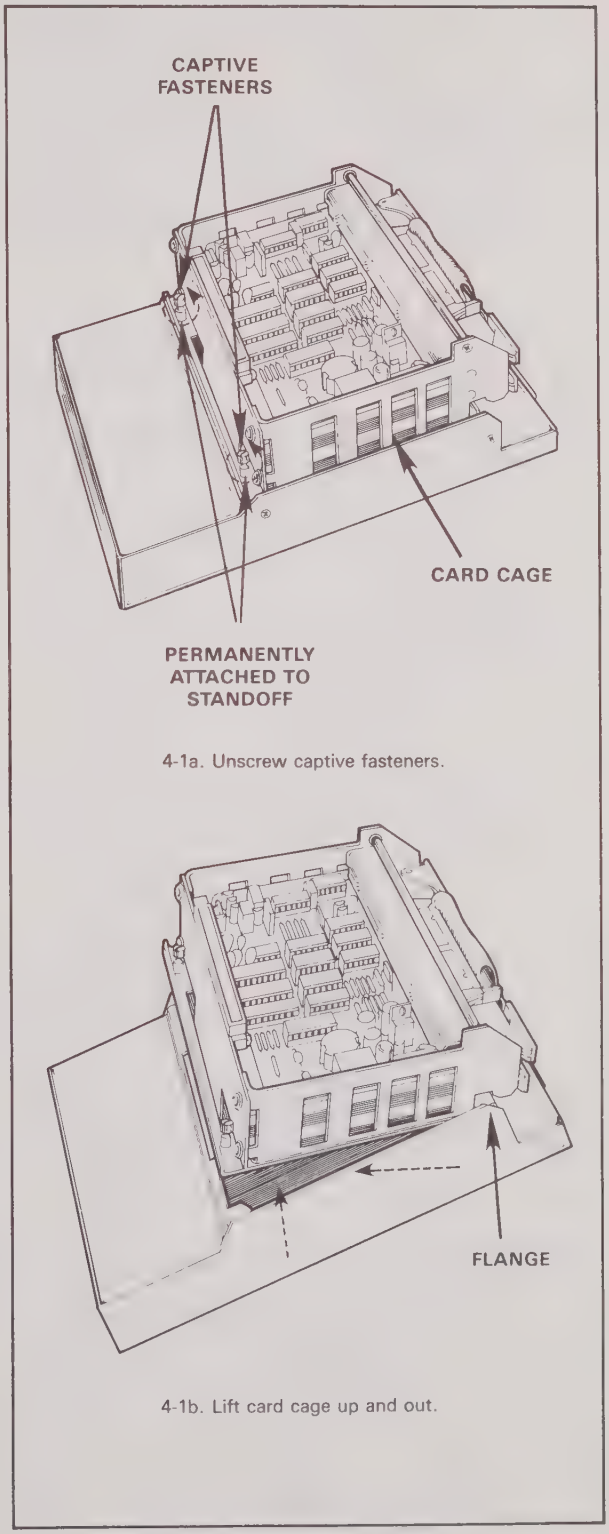


Figure 4-2. Socketboard Interconnect Cable Disconnect



4-1a. Unscrew captive fasteners.

4-1b. Lift card cage up and out.

Figure 4-1. GangPak™ Disassembly

6. Lift the extraction tabs out on each side of the connector (figure 4-2).
7. Pull the cable out of the connector.
8. Lift the extraction tabs out on the top card (waveform generator card) and unplug the interconnect cable from its connector (figure 4-3).
9. Flip the extraction tabs out on the top card (waveform generator card).
10. Pull the waveform generator card out along the guides (figure 4-3).
11. Repeat steps 9, 10, and 11 for the extraction tabs on the digital card.

4.2.2 Cleaning

Inspect the GangPak™ inside and out for accumulated dirt or dust. To clean the GangPak™, follow the procedure below.

1. Wipe any dust and/or dirt off the outside of the GangPak™ with a clean, damp cloth.

NOTE
Do not use abrasive cleaners or solvents that will etch the paint.

2. Remove dust from the circuit boards with a blast of dry, compressed air or a clean, soft-bristled brush.

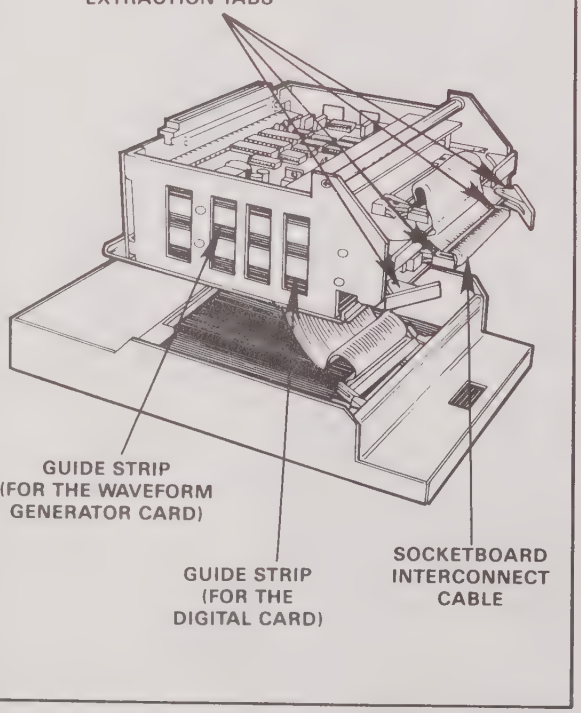

EXTRACTION TABS
GUIDE STRIP (FOR THE WAVEFORM GENERATOR CARD)
GUIDE STRIP (FOR THE DIGITAL CARD)
SOCKETBOARD INTERCONNECT CABLE

Figure 4-3. Circuit Board Removal

4.2.3 Inspection

You can help prevent malfunctions by periodically inspecting your GangPak™. Check cable connections, card seating, mounting of socketed components, etc., for shorts, opens, or unstable continuity.

If you find heat-damaged components, be particularly careful to find and correct the cause of the overheating. This will prevent further damage.

4.2.4 GangPak™ Assembly

1. Push the two extraction tabs down on the digital card.
2. Using the flat surfaces of the extraction tabs, gently push the digital card along the guides into its connector.
3. Make sure the extraction tabs on the interconnect cable connector are open.
4. Firmly, but gently, push the socket board interconnect cable into the connector. Notice that the extraction tabs will move back to their locked positions when the cable is locked into the connector.
5. Repeat steps 3 to 6 to replace the waveform generator card.
6. Plug the socket board interconnect cable into its connector on the socket board (figure 4-2).
7. Replace the card cage by tilting it up to lock the flanges, as shown in figure 4-1, then gently setting it down. Make sure the captive fasteners line up with the fastener holes on the GangPak™ frame.
8. Tighten the captive fasteners finger tight.

4.3 TROUBLESHOOTING

This section is intended to help you interpret and isolate failures in the GangPak™. It should be used in conjunction with section 5 (Circuit Description) and the schematics provided in the back of this manual.

There are three major classes of failures that can occur in a system comprised of a programmer and a GangPak™. The first is no system operation, the second is poor yields, and the third is GangPak™ failure.

After successfully troubleshooting the GangPak™, you must calibrate it according to the instructions in section 4.4. It is very important that the programmer be calibrated before the GangPak™ is calibrated.

4.3.1 No System Operation

The following steps should be performed if the system will not initialize with the GangPak™ installed. After completing each step, determine whether the problem still exists.

1. Check to be sure the GangPak™ is properly installed in your programmer.
2. Check the GangPak™ programmer mating connector (J1) for bent or broken pins. (Pin HH is intentionally shorter.)

3. Check the GangPak™ cards to be sure they are correctly installed in their connectors (section 4.2).
4. Check the ribbon cable to be sure it is properly inserted in the connectors (section 4.2).
5. Check the programmer power supplies for proper voltage output levels (see programmer manual).
6. If steps 1 through 5 fail to isolate the problem, contact your local Data I/O Service Center.

4.3.2 Poor Yields

The following steps should be performed if the yield rate begins to decrease. After completing each step, determine whether the problem still exists.

1. Perform a complete calibration, but be sure that the programmer has been calibrated first.
2. Perform waveform observations (section 4.4) for the family of the device being programmed, being careful to note any discrepancies. The Circuit Description (section 5) and the schematics at the end of this manual may be useful in isolating the problem.
3. Perform calibration steps 28 and 29 on the measurement chart for the device family that is giving problems. The Circuit Description (section 5), schematics, and suspected components in tests 1 through 4 of table 4-1 may be helpful in isolating the problem.
4. If steps 1 through 3 fail to isolate the problem, contact your local Data I/O Service Center.

4.3.3 GangPak™ Failure

The following steps should be performed if a device will not program at all or if error messages are displayed on the programmer. After completing each step, determine whether the problem still exists.

1. Check that the family and pinout codes are correct for the device, and that the device is being inserted in the socket correctly.
2. If possible, try a known-good device to determine whether it is a hardware problem.
3. Check to be sure the GangPak™ is properly installed.
4. Check the GangPak™ programmer mating (J1) connector for bent or broken pins. (Pin HH is intentionally shorter.)
5. Check the GangPak™ cards to be sure they are correctly installed in their connectors (section 4.2).
6. Check to be sure the ribbon cable is correctly oriented and properly inserted in the connectors.
7. Perform a complete calibration, noting any measurements falling outside the indicated limits. Refer to the corresponding test number in table 4-1 for suspected boards and components, as well as the Circuit Description (section 5) and the schematics, to help isolate the problem.
8. Perform waveform observations and note any discrepancies. Referring to the Circuit Desription and the schematics may be helpful in isolating the problem.
9. If steps 1 through 8 fail to isolate the problem, contact your local Data I/O Service Center.

4.4 CALIBRATION

The need for calibration varies with how much you use your GangPak™. Generally, we suggest calibration whenever: (1) programming yields fall below the manufacturer's recommended minimums; or (2) when troubleshooting has been completed; or (3) if your company policy requires periodic calibration certification.

NOTE

If calibration or repair is required but you lack the facilities to accomplish it, contact the nearest Data I/O Service Center.

Because of the different programmer mainframes, this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the GangPak™.

Calibration of the GangPak™ consists of three parts:

1. Power Supply Calibration—measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therfore, this part of the calibration procedure must be done first. Refer to your programmer manual.
2. DC Calibration—consists of measuring and adjusting critical DC voltage levels generated by the GangPak™.
3. Waveform Observation—enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

The first part of the calibration procedure (power supply calibration) varies with the type of programmer you have. Therefore, this manual refers you to your programmer manual for details on power supply calibration. DC calibration is discussed in section 4.4.1, the optional verify voltage checks are described in 4.4.2, and waveform observation is detailed in section 4.4.3. For information on how to carry out these steps on various programmers, consult your programmer manual.

The following equipment is necessary to calibrate the GangPak™.

- Data I/O Calibration Extender (part number 910-1521)
- Three and a half-digit digital voltmeter (DVM)
- Dual-trace Oscilloscope (Tektonrix 465 or equivalent)

Check the appropriate programmer manual for any additional equipment that you may need to calibrate the programmer.

Table 4-1. GangPak™ Troubleshooting Chart

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
1	701-0110 701-1822	VR3, R79, Q15, U5, U10, U13, U14, Q9, Q10, T1, U9 U18, U7
2	701-0110 701-1822	VR4, R82, Q15, U16, U5 U18, U7
3	701-0110	VR2, R59, Q15, U5
4	701-0110	U16, U5
5	701-0110	U6, U7, U8, U13, U17, U18, U2, U3, U4, Q2, Q3, Q4
6	-	U16, U5
7	-	U6, U7, U8, U13, U17, U18, U2, U3, U4, Q2, Q3, Q4
8	701-0109 701-0110	U3, U4, U8, U10, U12, U14, U16, U18, U20, U22 U12, U18
9	-	U16, U15
10	701-0110	Q9, Q10, U14, U9
11	701-0110	R58, Q6, U13, U14
12	701-0110	U11, U12, Q13, Q14, Q15
13	701-0110	U9, U11, Q5, U10, Q1
14	-	Q9, Q10, U14, U9
15	-	R58, Q6, U13, U14
16	701-0110	Q1, R56, R30, Q8, R50
17	701-0110	U7, U3, Q3, U17, U18, U13
18	701-0110	U3, Q3
19	701-0110	R16, Q17, R12
20	701-0110	U7, U3, Q3, U17, U18, U13
21	701-0110	R16, Q17, R12, U6, U2, Q2
22	702-0110	U8, U4, Q4
23	701-0110	U4, Q4
24	701-0110	R23, Q18, R19
25	-	U8, U4, Q4
26	701-0110	R23, Q18, R19, U6, U2, Q2
27	701-0110	U6, U2, Q2
28	701-0110	U2, Q2
29	701-0110	R9, Q16, R11
30	-	U2, U6, Q2
31	701-0110	R9, Q16, R11, U8, U4, Q4
32	701-0110	U12, U18
33	701-0109	U3, U4, U8, U10, U12, U14, U16, U18, U20, U22
34	701-0109	U3, U4, U8, U10, U12, U14, U16, U18, U20, U22

(more)

Table 4-1. (Continued)

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
35		
36	701-0110	U10, U11, U12
37	701-0109	U1, CR36, CR17
38	701-0109	U1, CR37, CR21
39	701-0109	U1, CR40, CR25
40	701-0109	U1, CR42, CR26
41	701-0109	U1, CR35, CR31
42	701-0109	U1, CR38, CR32
43	701-0109	U1, CR39, CR33
44	701-0109	U1, CR41, CR34
45	701-0110	R8, R73, R74, R27, U19
46	701-0110	VR3, R79, Q15, U5, U10, U13, U14, Q9, Q10, T1, U9
47	701-0110	VR4, R82, Q15, U16, U5, U6, U7, U8, U13, U17, U18, U2, U3, U4, Q2, Q3, Q4
48	701-0110	VR4, R82, Q15, U16, U5, U6, U7, U8, U13, U17, U18, U2, U3, U4, Q2, Q3, Q4

To prepare your GangPak™ for calibration, follow the procedures listed below.

1. Turn the programmer power off (see section 3.3 for details).
2. Remove the GangPak™ from the programmer (see section 2.3 for details).
3. Insert the calibration extender into the programmer the same way you insert the GangPak™ (see section 2.2).
4. Unscrew the two thumb screws (captive fasteners) located on the underside of the top cover of the GangPak™ (figure 4-1); they connect the card cage to the socket assembly. Separate the two parts of the assembly.

CAUTION

Do not let the fasteners short to the motherboard.

5. Insert the 64-pin connector of the card cage into the mating connector on the calibration extender (figure 4-4a).
6. Lean the top portion of the GangPak™ against its bottom portion at a 45-degree angle (see figure 4-4).

NOTE

Be sure the socket assembly flange locks into the card cage flange (see figure 4-4b).

Be careful not to strain the cable or scratch the top of the programmer.

4.4.1 DC Calibration

The DC calibration procedure described in this section enables you to adjust critical DC voltage levels generated by the GangPak™. To follow this procedure, see the measurement chart at the end of this section. This measurement chart contains the information necessary for all DC calibration tests. This information is included on the measurement chart (located at the end of section 4) in columns with the following headings:

- Step No.—tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No.—identifies individual tests.
- Test Description—identifies the functions being tested.
- Measurement Test Location—tells which socket pins, circuit boards, or test points to probe for measuring voltages.
- Measurement—specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the GangPak™ until the problem is corrected.
- Adjustment Location—tells which potentiometer to adjust if a measurement is out of range.
- Comments—gives special instructions for particular tests.

The DC calibration procedure is as follows:

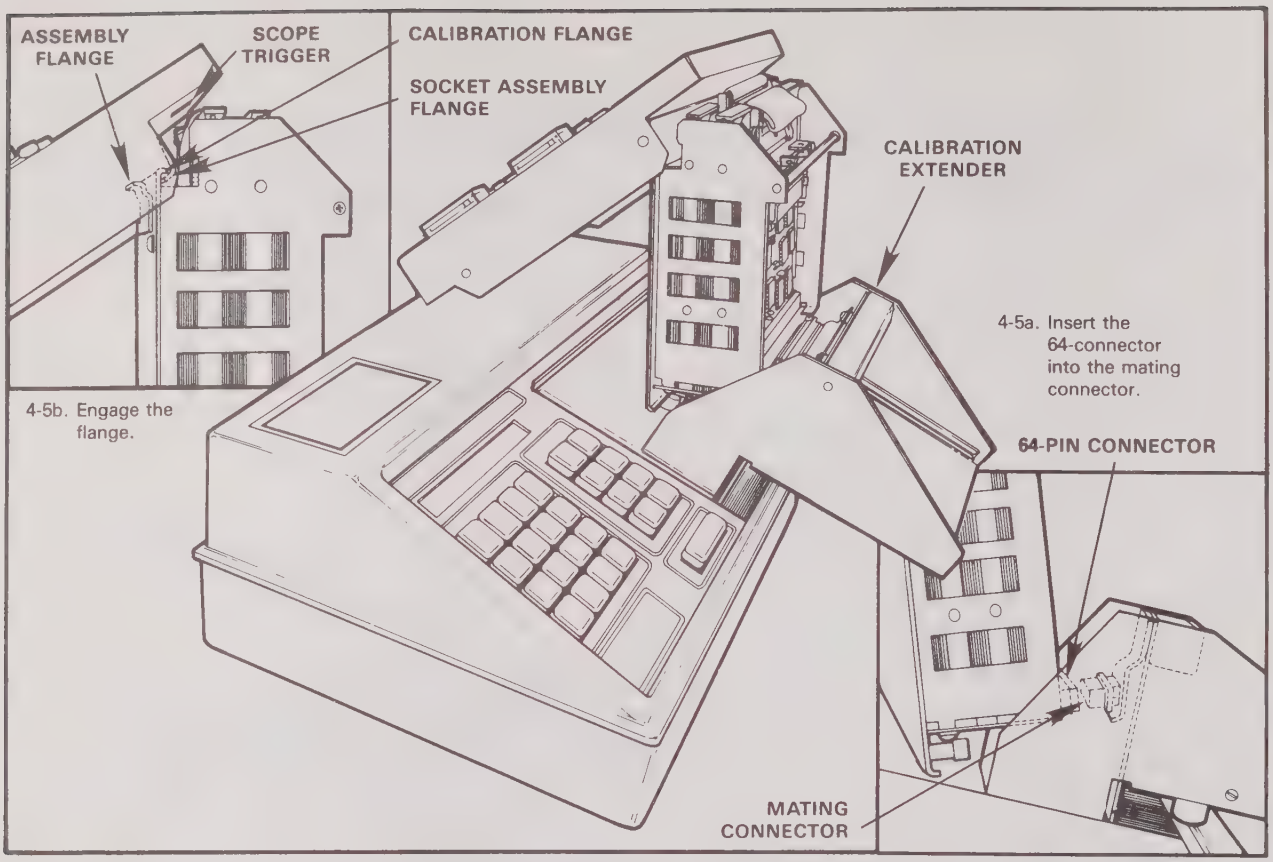


Figure 4-4. Calibration Setup

CAUTION

Remove all devices from the sockets before entering the calibration mode (see section 3.8 for details). Waveform generation may damage any device in the GangPak™ sockets.

1. Turn the programmer power on (section 3.2).
2. Put the programmer into the calibration mode by following the key sequences in table 4-2.
3. Perform the general calibration steps (step 1 through 27) on the measurement chart (Appendix A, table A-3). For steps 26 and 27, refer to the figures at the end of the measurement chart to observe the "V_{CC} sawtooth" "V_{PP} sawtooth," and the switching pin drivers.

Table 4-2. Key Sequence to Access the Calibration Mode

Programmer System	Key Sequence to Enter Calibration Mode	Increment Step No.	Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number (a) Press START	Enter	Review
29A	Press SELECT Press C1 Press START Enter Step Number (a) Press START	Start	Review
100A	Press SELECT Press 12 Enter Step Number (a) Press START	Start	Back-space

(a) Optional

For each general calibration step on the measurement chart do the following:

- Take measurement readings at the device sockets or test points indicated in the measurement chart; figure 4-5 shows the pin numbers for the sockets and figure 4-6 shows the test points.
- Ground the digital voltmeter to pin 14 of any socket on the front panel of GangPak™.
- The adjustment pots on the waveform generator enable you to make adjustments when your measurements do not match the measurement chart; figure 4-6 shows the location of these adjustment points.
- Access each new step by pressing the START (or ENTER) key. The new step number will appear on the display when the GangPak™ is ready for the next step. To go back to a previous test, press the REVIEW (or BACKSPACE) key.

NOTE

The remaining calibration (steps 28-33) are family-specific and can be performed optionally.

4. For each family-specific calibration step on the measurement chart, do the following to enter the family codes and pinout codes.
   - Enter the family code and pinout code when prompted by the programmer; refer to your programmer manual for further information.

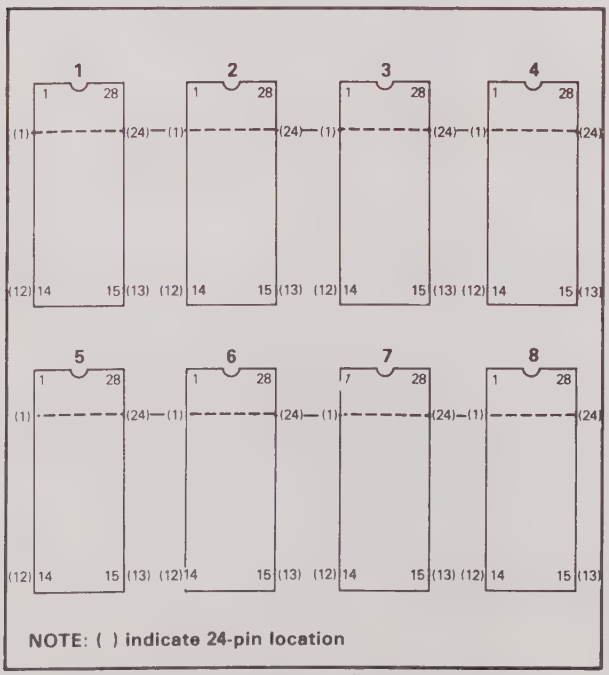


Figure 4-5. Pin Numbers of Device Sockets

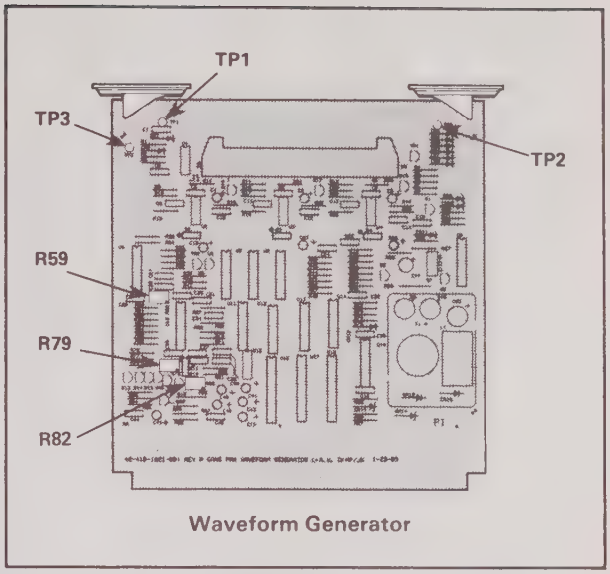


Figure 4-6. Adjustment Locations

- Put the programmer back into the calibration mode (see table 4-2 for the key sequence).
- Enter the step number from the measurement chart.
- Press START.

4.4.2 Optional Verify-Voltage Checks

Two calibration steps (28 and 29) have been provided for the measurement of first and second pass verify voltages. The family characteristics table in the applicable family timing diagram defines the levels for first and second pass verifications for each family. These are provided for the investigation of yield problems; no adjustments are available. Under normal circumstances, these steps can be eliminated from a routine calibration.

4.4.3 Waveform Observation

Programming waveforms of your GangPak™ can be observed with an oscilloscope and compared to the timing diagrams that have been provided at the end of this section. In this way, timing and magnitude relationships can be measured against known specifications to confirm that the GangPak™ is performing to the device manufacturer's specifications. Since the GangPak™ generates a large number of waveforms and all calibration adjustments are accomplished in DC calibration, it is necessary only to observe waveforms for commonly used devices or those that are presenting yield problems.

During the waveform observation phase of the calibration procedure, your GangPak™ uses a firmware routine that generates programming waveforms for the data stored in system RAM. An oscilloscope trigger pulse is generated for every address increment. The address is

automatically reset to Ø when the maximum PROM address is reached, and incrementing continues. Waveform observation can be done with the GangPak™ either on the calibration extender or plugged into the programmer.

When used with a timing diagram, this procedure allows you to compare waveforms on the oscilloscope with the waveform photographs on the timing diagram for any type of device; a detailed explanation of the timing diagrams is provided in section 4.4.4. The waveform observation procedure is as follows:

1. Refer to table A-1 to determine the family codes and pinout codes, polarity, and technology of the selected device.

NOTE

Polarity is indicated in the family code. Odd numbered families are VOL and even numbered families are VOH.

2. Initiate a load operation (see section 3.4 for details).
3. Key in family codes and pinout codes when prompted by the programmer (see section 3.4).

CAUTION

Remove all devices before entering the calibration mode. Waveform generation may damage any device in the GangPak™ sockets.

4. Enter the calibration mode by the appropriate key sequences listed in table 4-2.
5. Trigger your oscilloscope by connecting to the test point under the top edge of the socket assembly (see figure 4-7).
6. Ground the scope to pin 14 of any socket.
7. To observe individual waveforms, refer to figure 4-8 under the pinout code number entered in step 3. The individual socket illustrations give the numbers of the socket contacts to probe when observing the waveforms on the timing diagram.

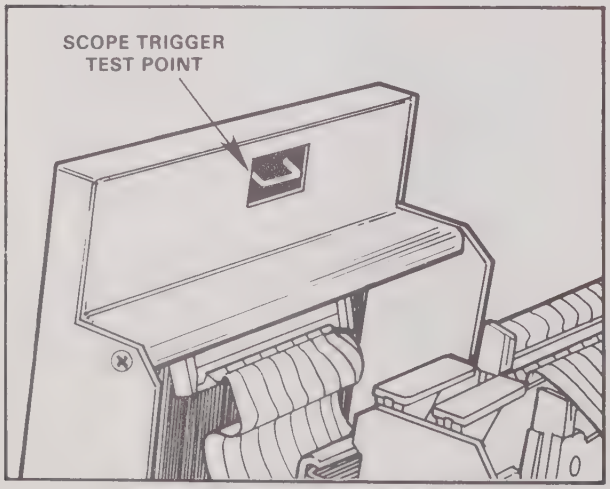


Figure 4-7. Scope Trigger Test Point

NOTE

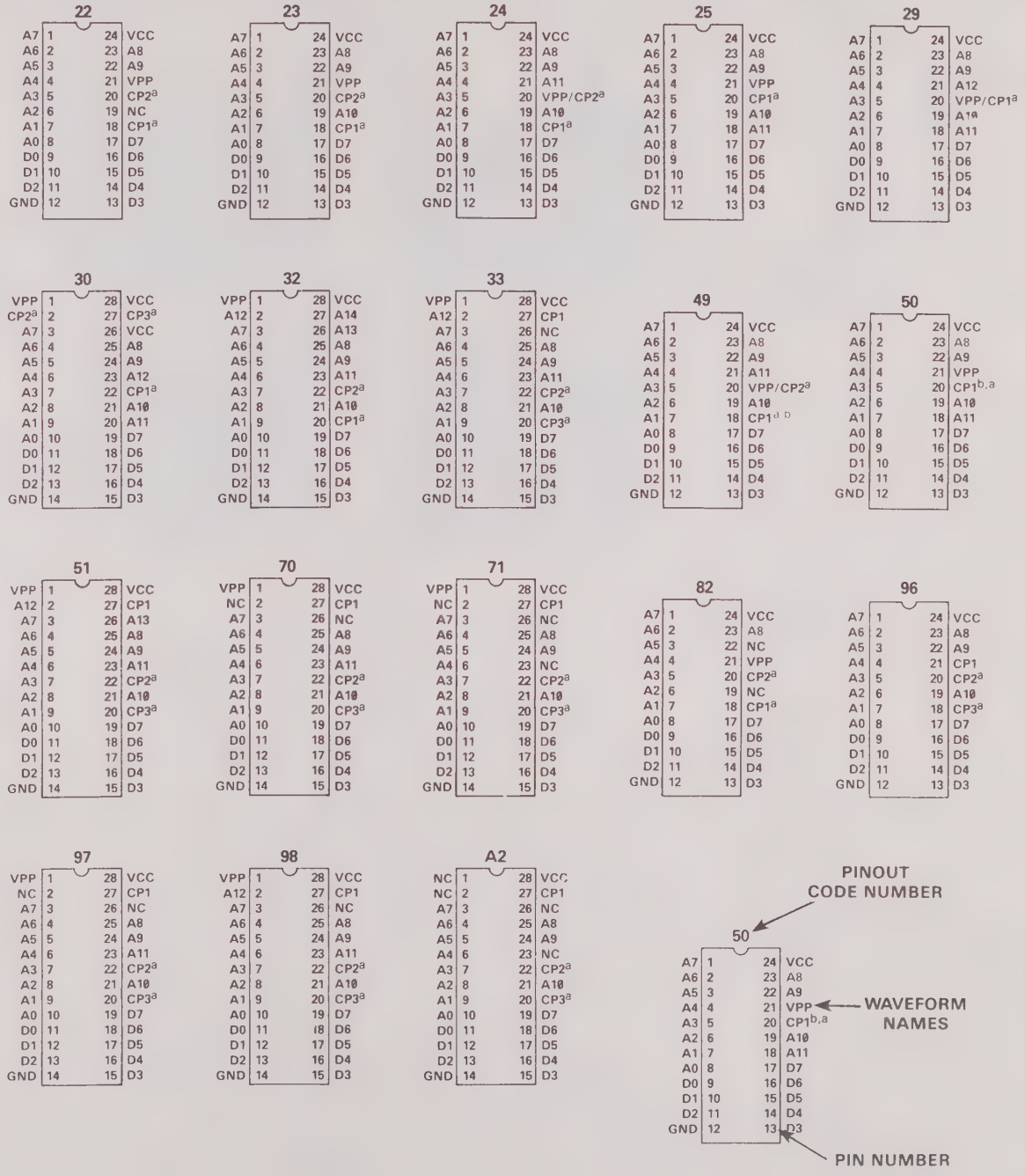
Considerations helpful in setting up and interpreting the waveform displays are explained in section 4.4.4.

4.4.4 Detailed Explanation of the Timing Diagrams

This manual contains a timing diagram for each device family that can be programmed by the GangPak™. Each timing diagram contains a set of waveform photographs that show critical programming parameters. To use these diagrams and photographs, read the information provided below and refer to the sample timing diagram (figure 4-9).

V_{PP} t_r and t_f photographs were taken with the volts-per-division uncalibrated. This was done to illustrate the t_r and t_f "10%-90%" points more clearly. This is indicated by the > symbol preceding the voltage displayed on the waveform photograph.

1. FAMILY CODE NUMBER—corresponds to the family code number of the device (refer to table A-1).
2. FAMILY CHARACTERISTIC TABLE—lists the minimum and maximum parameter values; voltage and timing parameters other than those listed in this table are to be considered non-critical with a ±10% tolerance.
3. NOTES—Important information pertaining to a timing diagram.
4. WAVEFORM NAMES—correspond to the pin names on the pinout chart (figure 4-8); the pinout chart tells you which socket pins to probe when you are observing the waveforms for a particular device pinout within a family. (The pinout is indicated by the number above each socket on figure 4-8 which corresponds to the pinout code on table A-1.)
5. LAYOUT SEQUENCE NUMBER—used as a reference point within each diagram.
6. DELAY TIME POSITION—indicates the time from the start of the main sweep to the start of the delay time.
7. OSCILLOSCOPE GROUND REFERENCE—identifies the ground level on a waveform.
8. TIME-BASE AND VOLTS-PER-DIVISION SETTINGS—horizontal positioning of the waveforms is not critical and may vary slightly from the photographs. The important observation is the timing relationship between the waveforms in the photographs. You can adjust this timing relationship on your oscilloscope to set convenient reference points. By taking into account any time-base variance, you can also make time comparisons between photographs. The time base is always the same for different waveforms in the same photograph.
9. VOLTAGE—indicates volts per division. The one in the upper left corner is for the top trace and the one in the lower left corner is for the bottom trace.



NOTES: [a] *Active low during read.*
[b] *Clocked during read for address latches.*

Figure 4-8. Pin Names by Pinout Code Numbers

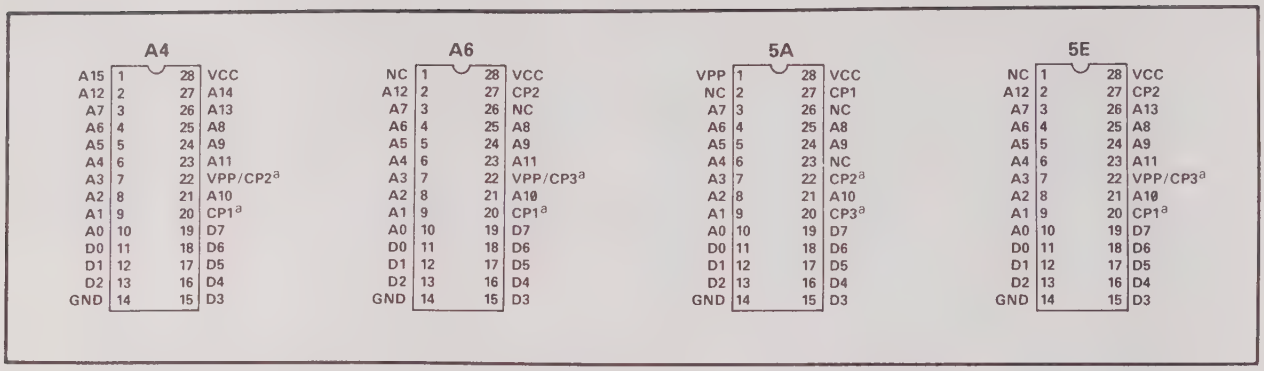


Figure 4-8. Pin Names by Pinout Code Numbers (Continued)

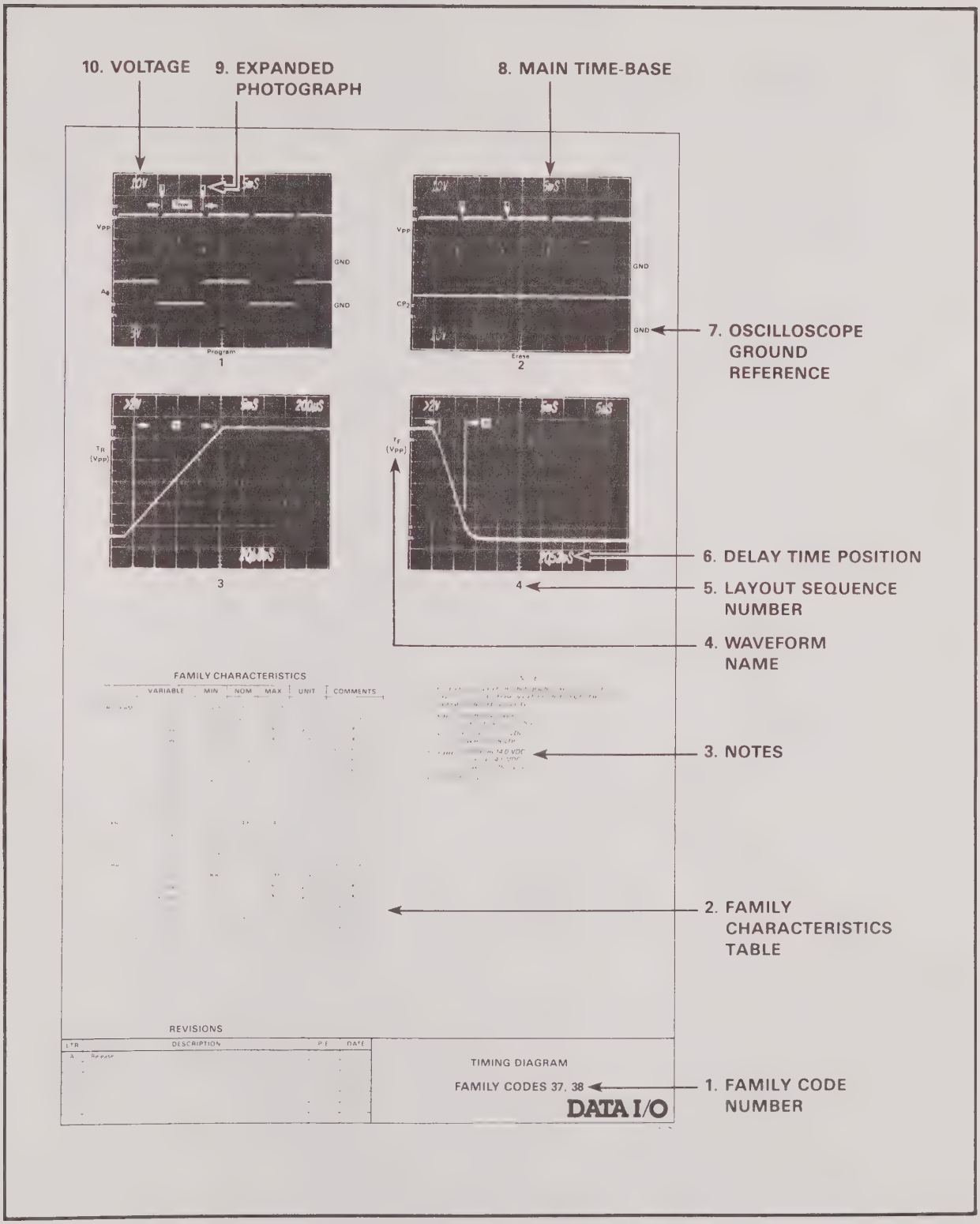


Figure 4-9. Sample Timing Diagram

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SECTION 5
CIRCUIT DESCRIPTION

5.1 OVERVIEW

This section defines the functions of the GangPak™'s principal hardware components. Each circuit card assembly is depicted by a block diagram accompanied by a written description.

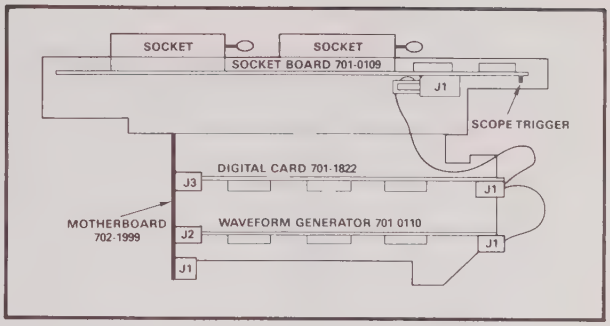


Figure 5-1. Principal Components

5.2 GENERAL ARCHITECTURE/ COMPONENT LAYOUT

The GangPak™ is controlled by the programmer's extended processor bus through the mating connector (J1 on Figure 5-1). The control software for the GangPak™ is located in EPROM on the digital card (701-1822).

The principal components of the GangPak™ are the motherboard, the waveform card, the digital card, and the socket card. The component layout of the GangPak™ is shown in figure 5-2 and described in the following subsections.

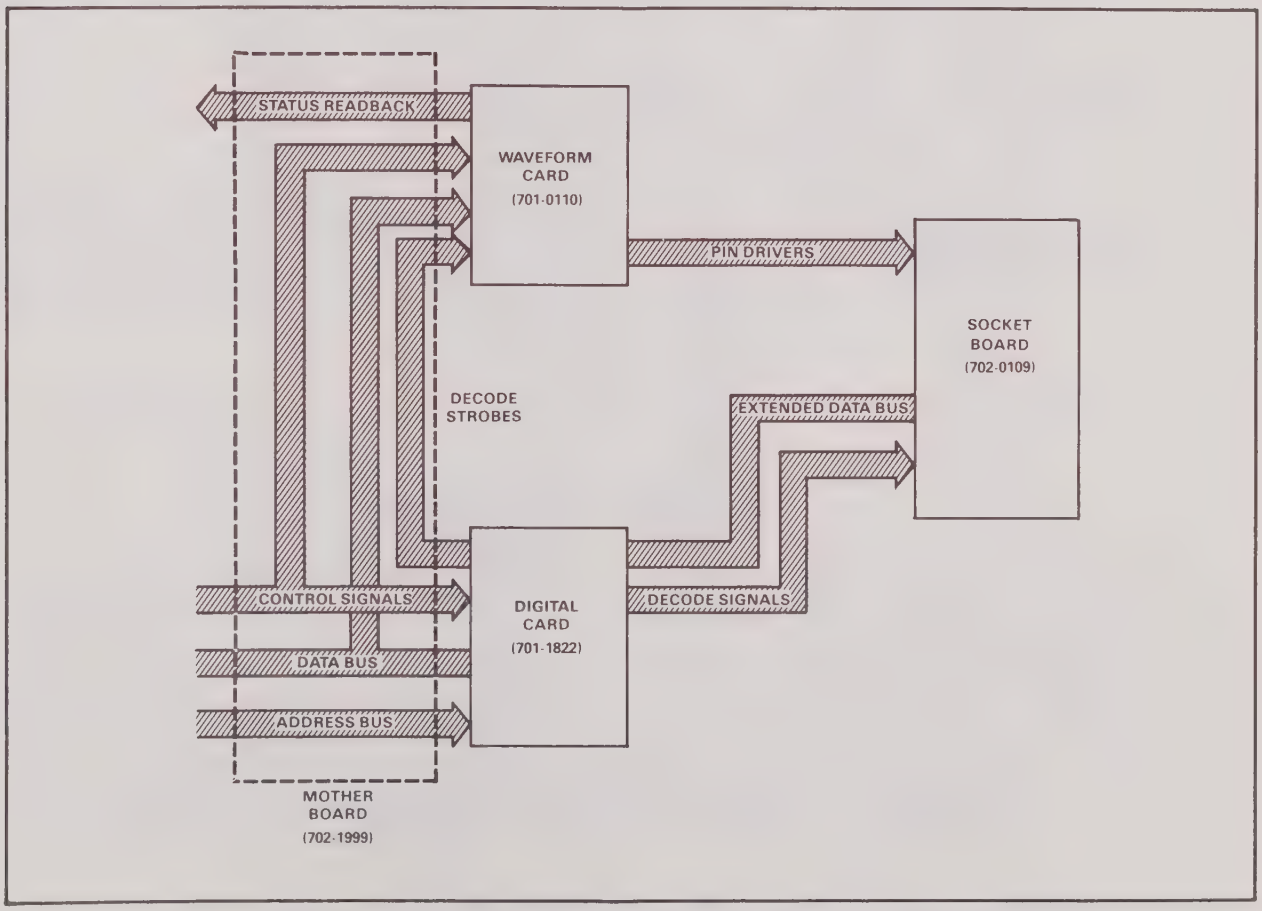


Figure 5-2. Block Diagram, GangPak™ Electronics

5.2.1 Digital Card

The digital card (shown in figure 5-3) provides the decode signals and software for the GangPak™. Decoding is accomplished with a PROM, a three-to-eight-line decoder and AND gates connected to the 15 high-order address lines and the write/read line. The signals used in decoding are first conditioned with transparent latches to ensure stable levels. Edge-sensitive decode strobes are conditioned with "OR" gates utilizing the system clock ($\overline{V02}$). The gate enable control block (figure 5-3) consists of a programmable logic array and an octal latch. This block works in conjunction with the data gate write/read control lines to allow selection of one of the eight socket board data gates to be read. The extended data bus is buffered on this card by a transceiver. The software to control the GangPak™ is contained in a single 8K PROM with expandability to 16K bytes.

5.2.2 Socket Card

The socket card (shown in figure 5-4) provides device addressing, device data gating, backward device test gating, a distributes the signals generated by the waveform generator card. The device address from A0 to A10 is generated by a pair of octal latches connected to all sockets in parallel. Address line A9 also has the capability to be switched to the super voltage level provided by the waveform card.

The unused portion of the high-order address driver is used to select a device for backward device testing. When the device test mode is activated, pin 25 on all sockets is individually disconnected from the address latch circuitry. Backward device sensing circitry on the waveform card is multiplexed to this pin on the selected device.

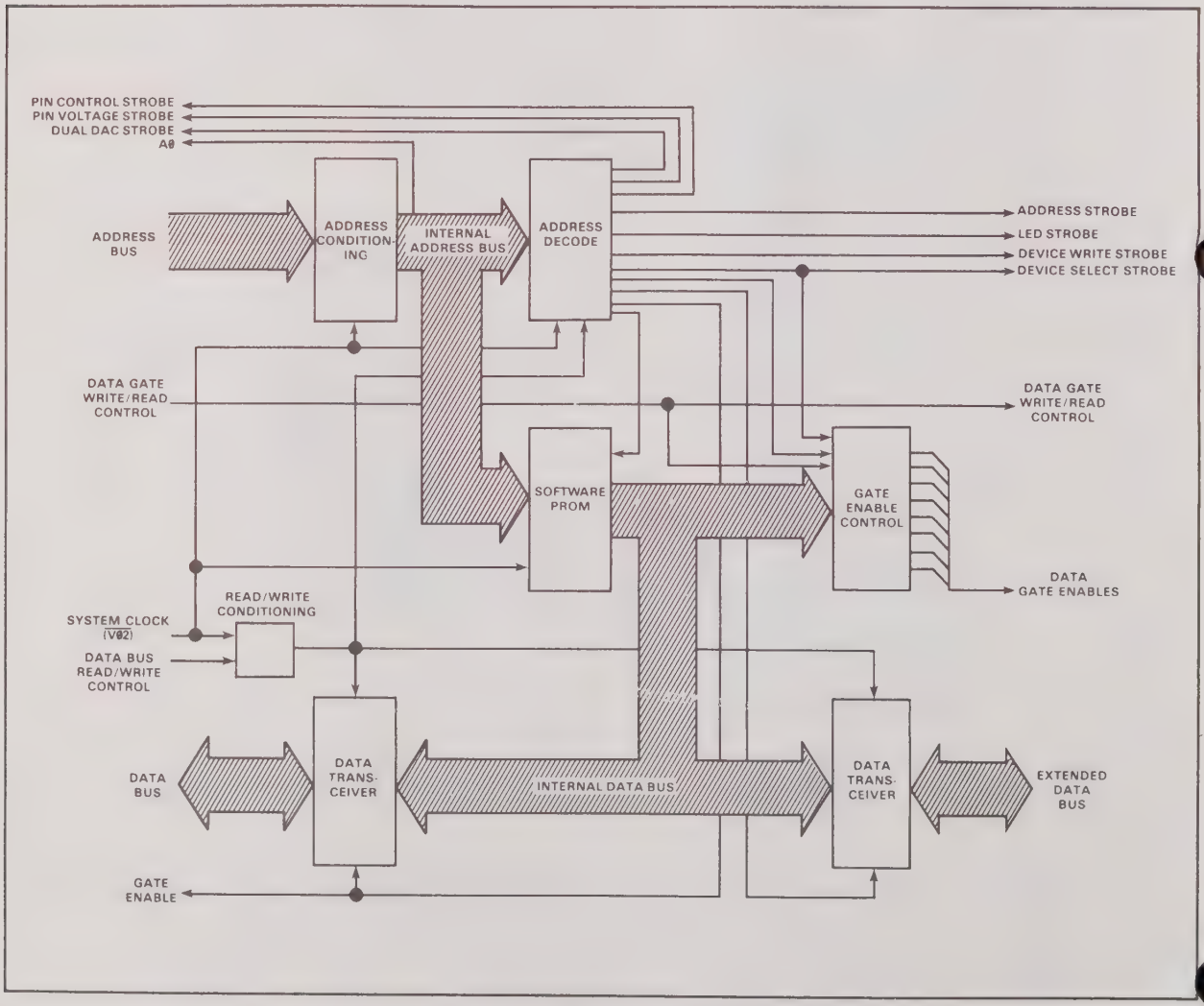


Figure 5-3. Block Diagram, Digital Card (701-1822)

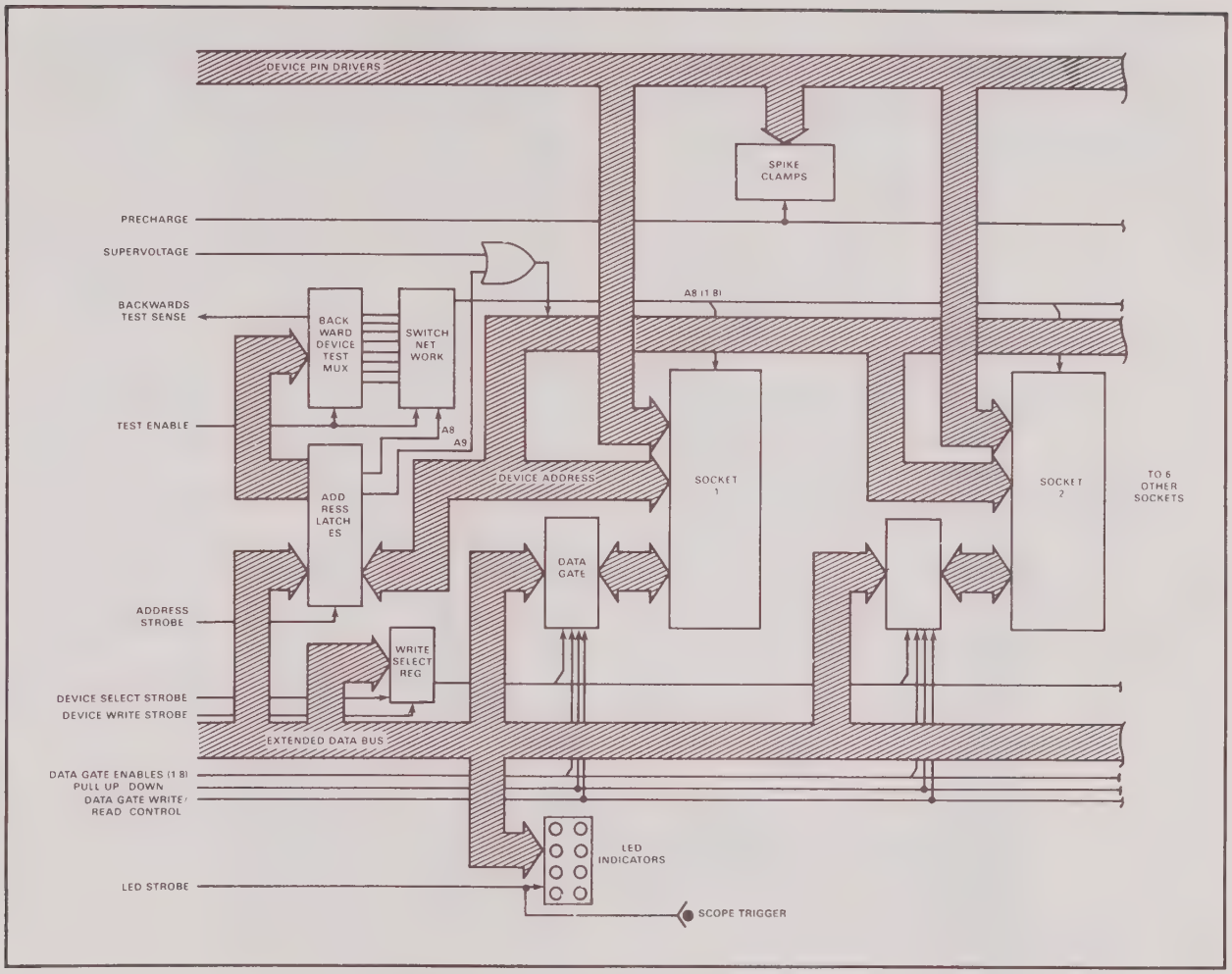


Figure 5-4. Block Diagram, Socket Board (701-0109)

As can be seen in Figure 5-4, an individual data gate is provided for each socket. The data gate consists primarily of a bi-directional, latched transceiver configured for two modes of operation. Data can be latched to the socket or data from the socket can be output to the extended data bus. When in the write mode, the write select register provides the clock pulse to latch data into the appropriate data gate. The mode is selected by the state of the data gate write/read control line. This control line is a latched signal that orginates from a register in the programmer.

When in the read mode, data from the selected socket is strobed onto the extended data bus when its enable is activated. This enable is generated on the digital card.

The pin driver outputs are distributed to each socket in parallel, as shown in figure 5-4. Spike suppression circuitry is provided on the socket card for pin drivers 1, 22, and 23. The capacitor in the spike clamp circuitry is charged by the precharge line to a level above which spikes will be suppressed.

5.2.3 Waveform Card

The waveform card supplies the voltage needed to power and configure the PROMs inserted in sockets on the socket card. The primary components of the waveform card are the pin driver circuits, overcurrent shutdown and reference generators, backward and register test circuitry, device data line pull-up/pull-down circuitry and the supervoltage circuitry (see figure 5-5). There are three basic types of pin drivers, characterizable by their output. These are the logic pin drivers, multivoltage pin drivers, and V_{CC} pin drivers.

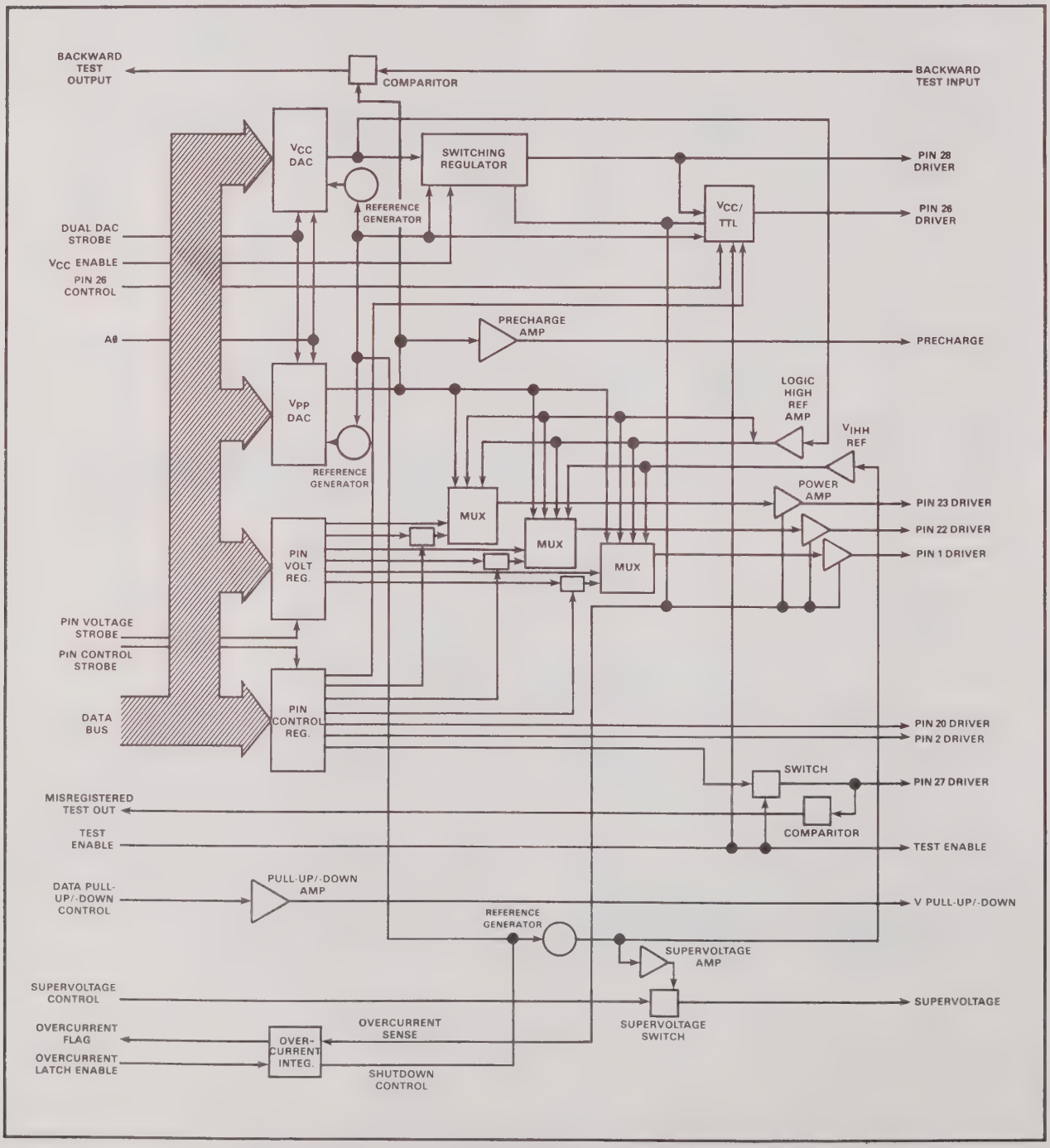


Figure 5-5. Block Diagram, Waveform Generator (701-0110)

Pins 2, 20, and 27 comprise the logic pin drivers. Logic levels for these pins are directly generated by the pin control register.

The multivoltage pin drivers are composed of pins 1, 22, and 23. These pins are programmable to four different levels: Ø logic low, logic high (V_{CC} DAC), V_{IHH} (+14.5 volts) and the V_{PP} (25.5 volts) DAC output. Switching between these levels is accomplished by the multiplexer (MUX) which is controlled primarily by the pin volt register (see figure 5-5). Two bits within the pin volt register are used to select which reference level is to be connected to the power amplifier output stage of the pin driver. The logic low and V_{IHH} are fixed references, while the V_{PP} and logic high references are programmable. The logic high reference level tracks the output of the V_{CC} supply. "OR" gates are used to merge the outputs of the pin volt and pin control registers to allow logic-level control of these pins by either register.

Pins 26 and 28 comprise the V_{CC} pin drivers. V_{CC} voltages are generated by a switching regulator that is programmable by the V_{CC} DAC output. Pin 28 always carries the output of the switching regulator. Pin 26, however, can supply either the output of the switching regulator or a logic level output, depending on the state of the pin 26 control line. This control line originates from a register in the programmer. When the switcher output is selected for pin 26 its output pull-up transistor (Q7) is staturated and feedback for the pulse width modulator is sensed at pin 26's output. When logic levels are desired on pin 26, the pulse width modulator receives its feedback from the pin 28 output while pin 26 output tracks the state of a bit in the pin control register.

Overcurrent conditions are sensed pin drivers 1, 22, 23, 26, and 28. These sense lines are routed to the overcurrent latch where they are integrated to disregard instantaneous current surges. Once an overcurrent condition has been detected, all reference generators are set to zero volts, thus shutting down the drivers.

Backward and misregistered device test circuitry operate using the same principle. The pin under test is pulled negatively and the resultant level is sensed. This level is compared to a fixed reference or, in the case of the backward test, a programmable level. Output from the comparators is routed to a buffer in the programmer, where they can be read by the processor.

The pull-up/pull-down amplifier (amp) provides the voltage for the data gate pull-up/pull-down resistors on the socket card. The amp tracks the output of a bit in a programmer register.

The supervoltage amp has a fixed output of +12 volts. Its output can be switched onto the supervolt line which is routed to the socket card. Once switched on, its output will override the output of the address driver on the socket card for pin 24. The switch is controlled by a register in the programmer.

BLANK

APPENDIX A
FAMILY CODES AND PINOUT CODES TABLE
AND
ERROR CODES

Table A-1. GangPak™ Family and Pinout Codes

Device Part Number	Family & Pinout Codes		Software Version	Approval Status
Advanced Micro Devices				
2716/AM9716	19	23	V01	A
2732/AM9732	19	24	V01	A
2732A	27	24	V01	S
2764/AM9764	AF	33	V01	A
	79	33	V05	S
2764A	C1	33	V05	S
27128	AF	51	V01	A
	79	51	V05	S
27128A	C1	51	V05	S
27256	C1	32	V04	S
27512	DD	A4	V05	S
9864	C9	A6	V05	S
Electronic Arrays				
2716	19	23	V01	S
Eurotechnique				
ET2716	19	23	V01	A
ETC2716	19	23	V01	A
ET2732	19	24	V01	A
Excel				
2816A	B7	23	V05	S
Fujitsu				
8516	19	23	V01	S
8532	19	24	V01	S
2732A	27	24	V01	S
2732A-35	27	24	V01	S
2764	45	33	V05	S
27C64	45	33	V05	S
27128	45	51	V05	S
27C128	45	51	V05	S
27256	45	32	V05	S
27C256	45	32	V05	S
	F7	32	V05	S
General Instruments				
5716	83	23	V01	S
5816	37	23	V01	S
Hitachi				
27C64	79	33	V05	S
462532	19	25	V01	S
462716	19	23	V01	S
462732	19	24	V01	S
462732P	19	24	V01	S
48016	33	23	V01	S
482732A	27	24	V01	S
482764	79	33	V05	S
4827128	79	51	V05	S
Intel				
2716	19	23	V01	A
2732	19	24	V01	A
2732A	27	24	V01	A
2732B	93	24	V04	S
2764	79	33	V05	A
2764A	93	33	V01	S
27128	79	51	V05	A
27128A	93	51	V01	S
27256	93	32	V01	A
27512	4B	A4	V05	S
27513	5B	5E	V05	S
2815	85	23	V01	A
2816	37	23	V01	A
2816A	A5	96	V04	S
2817A	BF	A2	V05	S
2864	A5	98	V04	S
Mitsubishi				
2716	19	23	V01	S
2732	19	24	V01	S
2732A	27	24	V01	S
2764	79	33	V05	S
27128	79	51	V05	S
Mostek				
2716	19	23	V01	O

Device Part Number	Family & Pinout Codes		Software Version	Approval Status
Motorola				
6836E16	2D	5A	V05	S
MCM2532	19	25	V01	A
MCM2716	19	23	V01	A
MCM2816	43	23	V01	A
MCM2817	81	71	V01	A
MCM2832	81	70	V01	A
MCM68764	25	29	V01	A
MCM68766	25	29	V01	A
National Semiconductor				
2532	19	25	V01	A
2716	19	23	V01	A
27C16	19	23	V01	A
27C16H	BD	23	V05	S
2732	19	24	V01	A
27C32	19	24	V01	A
27C32H	BD	24	V04	S
2758A	19	22	V01	A
2764	35	33	V01	A
2764H	63	33	V04	S
2816	37	23	V01	A
9716	B3	23	V01	A
Nippon Electric Company, Ltd.				
2716	19	23	V01	S
2732	19	24	V01	S
2732A	27	24	V01	S
2764	79	33	V05	S
27128	79	51	V05	S
Oki				
2532	19	25	V01	S
2716	19	23	V01	S
2732	19	24	V01	S
2732A	27	24	V01	S
2758	19	22	V01	S
2764	79	33	V05	S
27128	79	51	V05	S
Ricoh				
RD5H32	27	24	V01	S
Rockwell				
5213	A5	96	V04	S
R2816A	A5	96	V04	S
R87C32	27	24	V01	S
R87C64	35	33	V01	S
Seeq				
27C256	93	32	V01	S
2816A	B7	23	V05	S
5133	35	33	V01	A
	79	33	V05	A
5133H	79	33	V05	A
5143	35	51	V01	S
	79	51	V05	S
5213	A5	96	V01	S
5213H	B9	96	V04	S
52B13	A5	96	V01	S
52B13H	B9	96	V04	S
52B23	AB	97	V04	S
52B23H	AB	97	V04	S
52B33	AB	98	V04	S
52B33H	AB	98	V04	S
5516A	B7	23	V05	S
SGS				
2716	19	23	V01	S
Signetics				
27C64	35	33	V01	S
Texas Instruments				
2516	19	23	V01	A
	BD	23	V05	S
2532	31	25	V01	A
	BD	25	V05	S
25L32	19	25	V01	S

Table A-1. GangPak™ Family and Pinout Codes (Continued)

Device Part Number	Family & Pinout Codes		Software Version	Approval Status
Texas Instruments (Continued)				
2564	31	30	V01	A
	BD	30	V05	S
2732	31	24	V01	A
2732A	27	24	V01	S
	63	24	V05	S
2764	35	33	V01	A
	79	33	V05	S
27128	35	51	V01	S
	79	51	V05	S
Toshiba				
323	19	23	V01	S
2732	19	24	V01	S
2732A	27	24	V01	S
2732D	19	24	V01	S
2764	79	33	V05	S
27128	79	51	V05	S
57256	45	32	V05	S
VLSI Technology				
27C64	35	33	V01	S
Xicor				
2804A	B7	82	V05	S
2816A	B7	23	V05	S
2864A	C3	98	V05	S

KEY TO HEADINGS AND FOOTNOTES

- **Device Part Number.** The number assigned by the device manufacturer.
- **Family Code.** A 2-digit number that designates the programming algorithm.
- **Pinout Code.** A 2-digit number used to differentiate device types based on pin assignment and array size.
- **Software Version.** A number in this column that specifies the earliest software version of the GangPak™ that will program the device to the manufacturer's latest specifications.
- **Approval Status.** The following is an explanation of the symbols used in this column:

  A - Written approval obtained.

  O - Device is obsolete and no longer in production. No approval can be obtained. Algorithm has been used and approved in previous Data I/O equipment.

  S - This algorithm is in the process of submittal for manufacturer approval. The algorithm has been tested by Data I/O or the manufacturer, but no representation as to yield level is made or implied.

CAUTION

Entry of an invalid family/pinout code—one other than those listed in this table—can cause unpredictable results at the device socket, which may damage a device. A valid family code and a valid pinout code may be combined to produce an invalid (illegal) combination. The correct combination for your device is published in this table. All family/pinout combinations not contained in this table are considered "illegal." Data I/O assumes no responsibility or liability for results produced by entry of "illegal" family/pinout combinations.

Table A-2. Error Codes

CODE	NAME	DESCRIPTION	CORRECTIVE ACTION
21	Illegal-Bit	The device has previously programmed bits of opposite polarity to programming data.	Remove device and erase it.
23	First-Pass Verify	The device data was incorrect on the first pass of of the automatic verify sequence during device programming.	Remove device(s) that failed and reverify the rest.
24	Second-Pass Verify	The device data was incorrect on the second pass of the automatic verify sequence during device programming.	--
27	Insufficient RAM	RAM required for the operation exceeds the available amount.	Check for correct begin-RAM address, word count of device or block size selected, and set size and word size.
31	Excessive Current Drain	The operation aborted due to excessive current drain by a device.	Remove devices. If problem persists, a hardware failure may have occurred that requires servicing.
32	Backward Device	The operation aborted due to a device being inserted upside down.	Reinsert backward device.
35	Faulty Chip Select	The operation aborted due to device data drivers being still active when device chip enables de-selected.	Remove device. If problem persists, a hardware failure may have occurred that requires servicing.
38	Illegal Calibration Operation	Nonexistent calibration step number or calibration step invoked without family code and/or pinout code selected.	See calibration chart for proper operational procedures.
63	Faulty Load	Device data failed to transfer to RAM correctly.	Repeat load operation.
98	Incorrect Block Size	Block size selected exceeds word count of the device.	Reset block size value.
A1	No ID Found	The device does not have an electronic identifier.	Operations using this device require normal family and pinout code entry.
A2	Invalid ID	This device has an electronic identifier which is incompatible with the other inserted devices or has an unrecognized electronic identifier.	Remove violating devices(s).
A3	Address Out-of-Bounds	Address selected to be edited was outside the selected block limits.	Reset the block limit size or select an address within the present block limits.
A6	Misregistered Device	A 24-pin device has been inserted that is making contact with the upper portion of the socket.	Be sure that all devices have been properly inserted. If the error occurs when a 28-pin device is inserted, check to be sure the correct family and pinout codes have been used.

Table A-2. Error Codes (Continued)

CODE	NAME	DESCRIPTION	CORRECTIVE ACTION
A7	Incorrect Set Word Size Combination	Set size (automatically calculated during load or selected manually) and word size combination exceeds units capabilities.	Check for correct set size and word size selections.
A8	Incorrect Family Code and/or Pinout Code	Improperly selected family code and/or pinout code.	Refer to the family and pinout code (table A-1) for correct device code.
A9	Illegal Insertion	A device has been inserted in a socket that must be empty.	Remove device(s) that are in the wrong socket(s).

Table A-3.

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release		

GangPak™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION CIRCUIT SOCKET PIN BOARDS/TEST POINTS	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
			The following test is performed with					
			the GangPak™ on the calibration extender:					
1	1	Reference calibrate	701-1821/TP1	-3.42	-3.37	-3.32	R59,701-1821	
	2	V_{PP} calibrate	701-1821/TP3	-5.15	-5.10	-5.05	R82,701-1821	
	3	V_{CC} calibrate	701-1821/TP2	4.95	5.00	5.05	R79,701-1821	
			The remaining tests are performed with					
			the GangPak™ installed in its normal					
			operating position:					
2	4	V_{CC} linearity check	2/28	10.90	11.00	11.10		
	5	V_{PP} linearity check	2/1,22,23	14.90	15.00	15.10		
3	6	V_{CC} linearity check	2/28	2.90	3.00	3.10		
	7	V_{PP} linearity check	2/1,22,23	5.90	6.00	6.10		
4	8	Cold socket test	All/All	-0.10		0.40		Note that all LEDs are off. Error indicated if socket data lines are not tristate. LED's indicate problem sockets.
5	9	V_{CC}	All/28	6.60	6.70	6.80		
	10	V_{CC} load	2/28	6.40				Connect a 5Ω ±5%, 10W resistor between pins 28 and 14 of socket 2.

Table A-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release		

GangPak™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION CIRCJIT SOCKET PIN / BOARDS/TEST POINTS	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
5	11	V_{CC} overcurrent						Briefly touch a 2Ω ±10%, 5W resistor between pins 28 and 14 of socket 2. Note: beeps and LEDs flash.
	12	Overcurrent shutdown	A11/A11	-0.10		0.40		
6	13	Pin 26 V_{CC}	A11/26	6.60	6.70	6.80		
	14	Pin 26 V_{CC} load	2/26	6.40				Connect a 5Ω ±5%, 10W resistor between pins 26 and 14 of socket 2.
	15	Pin 26 V_{CC} overcurrent						Briefly touch a 2Ω ±10%, 5W resistor between pins 26 and 14 of socket 2. Note: beeps and LEDs flash.
7								
	16	Pin 26 sink overcurrent						Briefly touch a 25Ω ±10%, 5W resistor between pins 26 and 28 of socket 2. Note: beeps and LEDs flash.
8								
	17	Pin 1 V_{PP}	A11/1	17.90	18.00	18.00		
	18	Pin 1 V_{PP} load	2/1	17.80				Connect a 50Ω ±5%, 10W resistor between pins 1 and 14 of socket 2.

Table A-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release		

GangPak™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION CIRCUIT SOCKET PIN BOARDS/TEST POINTS	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
8	19	Pin 1 Vpp overcurrent						Briefly touch a 25Ω ±10%, 5W resistor between pins 1 and 14 of socket 2. Note: beeps and LEDs flash.
9	20	Pin 1 V_{IHH}	2/1	14.00	14.50	15.00		
	21	Pin 1 sink overcurrent						Touch a 3300Ω ±5%, 1/4W resistor between pins 1 and 23 of socket 2. Note: beeps and LEDs flash.
10	22	Pin 22 Vpp	A11/22	17.90	18.00	18.10		
	23	Pin 22 Vpp load	2/22	17.80				Connect a 50Ω ±5%, 10W resistor between pins 22 and 14 of socket 2.
	24	Pin 22 Vpp overcurrent						Briefly touch a 25Ω ±10%, 5W resistor between pins 22 and 14 of socket 2. Note: beeps and LEDs flash.
11	25	Pin 22 V_{IHH}	2/22	14.00	14.50	15.00		

Table A-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release		

GangPak™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION CIRCUIT SOCKET PIN BOARDS/TEST POINTS	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
	26	Pin 22 sink overcurrent						Touch a 3300Ω ±5%, 1/4W resistor
								between pins 22 and 23 of socket
								2. Note: beeps and LEDs flash.
12	27	Pin 23 Vpp	All/23	17.90	18.00	18.10		
	28	Pin 23 Vpp load	2/23	17.80				Connect a 50Ω ±5%, 10W resistor
								between pins 23 and 14 of
								socket 2.
	29	Pin 23 Vpp overcurrent						Briefly touch a 25Ω ±10%, 5W
								resistor between pins 23 and 14
								of socket 2. Note: beeps and
								LEDs flash.
13	30	Pin 23 V_{IHH}	2/23	14.00	14.50	15.00		
	31	Pin 23 sink overcurrent						Touch a 3300Ω ±5%, 1/4W resistor
								between pins 22 and 23 or socket
								2. Note: beeps and LEDs flash.
14	32	Address, data and	All/2,4,6,8,10,12,15,17,19,	4.00		5.50		
		controls high	21,23,25,27					
	33	Address, data and	All/1,3,5,7,9,11,13,16,18,20,	-0.10		0.40		
		controls low	22,24,26,28					

Table A-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release		
B	ECN 4926	[illegible]	10/11/83

GangPak™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION CIRCUIT SOCKET PIN BOARDS/TEST POINTS	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
15	34	Address, data and	A11/2,4,6,8,10,12,15,17,19	-0.10		0.40		
		controls low	21,23,25,27					
	35	Address, data and	A11/1,3,5,7,9,11,13,16,18,20,	4.00		5.50		
		controls high	22,24,26,28					
16	36	A9 supervoltage	2/24	11.80	12.00	12.20		
17	37	Device 1 backward						Note lighted LED on socket 1.
								Note beeps and flashing LEDs
								when 470Ω ±5%, 1/4W resistor is
								connected between pins 25
								and 14 of socket 1.
18	38	Device 2 backward						Same as step 17, except socket 2.
19	39	Device 3 backward						Same as step 17, except socket 3.
20	40	Device 4 backward						Same as step 17, except socket 4.
21	41	Device 5 backward						Same as step 17, except socket 5.
22	42	Device 6 backward						Same as step 17, except socket 6.
23	43	Device 7 backward						Same as step 17, except socket 7.
24	44	Device 8 backward						Same as step 17, except socket 8.

Table A-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release		

GangPak™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION CIRCUIT SOCKET PIN BOARDS/TEST POINTS	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
25	45	Misregistered device						Note beeps and flashing LEDs when 470 Ω ±5%, 1/4W resistor is connected between pins 27 and 14 of socket 1.
26	46	V_{CC} sawtooth	2/28					Connect a 100 Ω ±10%, 1W resistor between pins 28 and 14 of socket 2. Observe waveform as shown on last page of this table.
	47	V_{PP} sawtooth	2/1,22,23					Observe waveform as shown at end of this table.
27	48	Switching Pin Drivers	2/1,22,23					Observe waveform photo (at end of this table).
			The following tests are used for verification of particular family and pinout characteristics and are not required for calibration.					
28	49	Static first pass verify levels						See family characteristics table associated with the selected family timing diagram.

Table A-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release		

GangPak™ Measurement Chart

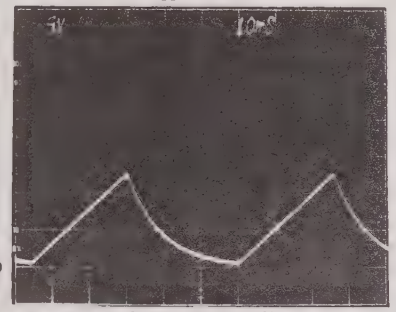
STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION CIRCUIT SOCKET/PIN BOARDS/TEST POINTS	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
29	50	Static second pass verify levels						See family characteristics table associated with the selected family timing diagram.
30	51	Static program inhibit levels						See family characteristics table associated with the selected family timing diagram.
31	52	Address increment loop						Address bus of selected pinout is incremented approximately every 100 µs.
32	53	Programming waveforms						See waveforms for selected family
33	54	Erase waveforms						See waveforms for selected family
								Fatal error if non-electrically-erasable family selected.

Measurement Chart

PROGRAM ELECTRONICS GANG PAK™

DATE	REV	REVISION RECORD	DR	CK
5/26/83	A	Release	DG	BL

V_{CC} SAWTOOTH

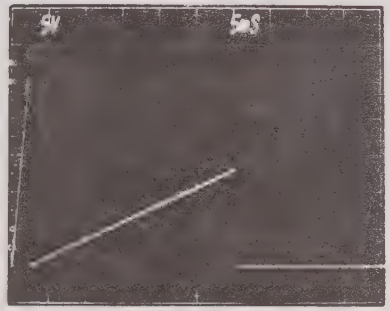


CALIBRATION STEP 26

A. VCC Sawtooth

1. *Check linearity.*
2. *Check continuity.*
3. *Final voltage = 12.5V ± 1V.*

V_{PP} SAWTOOTH

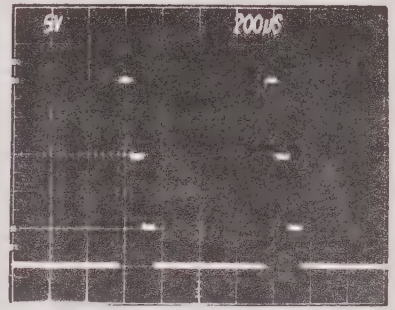


CALIBRATION STEP 26

B. VPP Sawtooth

1. *Check linearity for high ramp.*
2. *Check continuity for high ramp.*

SWITCHING PIN DRIVERS



CALIBRATION STEP 27

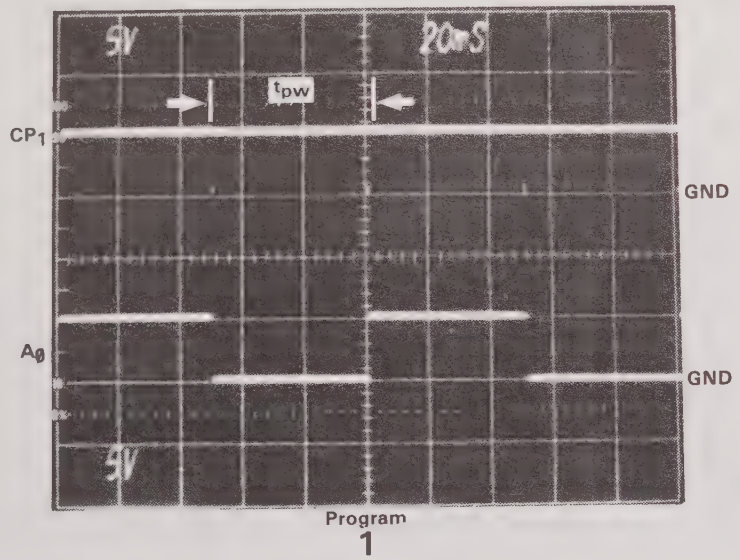
C. Switching Pin Drivers

1. *Verify that the top, middle, and bottom steps are present.*
2. *Rise time to top step is less than 5μ sec (10% - 90%).*
3. *Low step voltage = 5.0V ± .1V.*

BLANK

TIMING DIAGRAMS FOR FAMILY CODES

19, 1A
25, 26
27, 28
2D, 2E
31, 32
33, 34
35, 36
37, 38
43, 44
45, 46
4B, 4C
5B, 5C
63, 64
79, 7A
81, 82
83, 84
85, 86
93, 94
A5, A6
AB, AC
AF, B0
B3, B4
B7, B8
B9, BA
BD, BE
BF, C0
C1, C2
C3, C4
C9, CA
DD, DE
F7, F8


5V
20mS
tpw
CP1
GND
Aø
GND
5V
Program
1

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IH}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	48		52	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IL}.*

REVISIONS

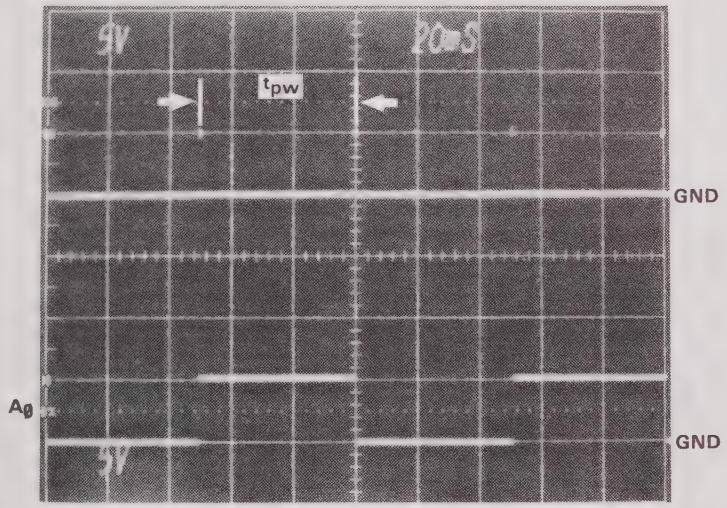
LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/18/83

TIMING DIAGRAM

FAMILY CODES 19, 1A

DATA I/O

0526\1282



1

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IL}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	48		52	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	
	t_f (V_{PP})				µsec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *This Family Characteristics table is to be used with pinouts 24, 25, 49 & 50. All other pinouts see sheet 1.*

REVISIONS

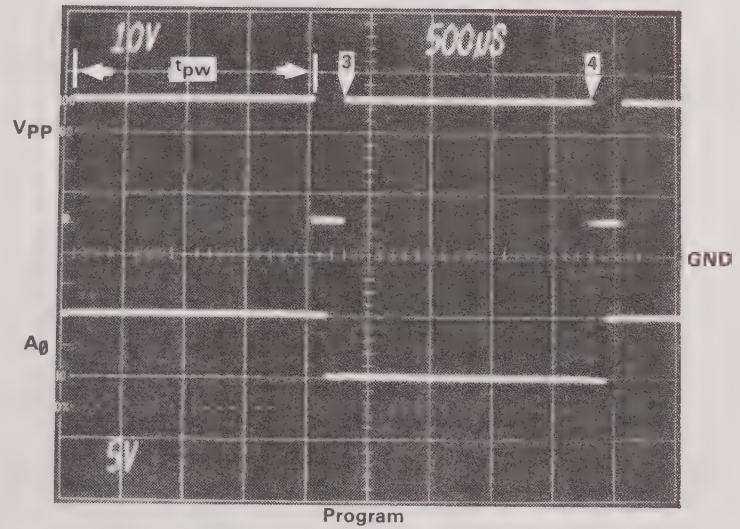
LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/18/83

TIMING DIAGRAM

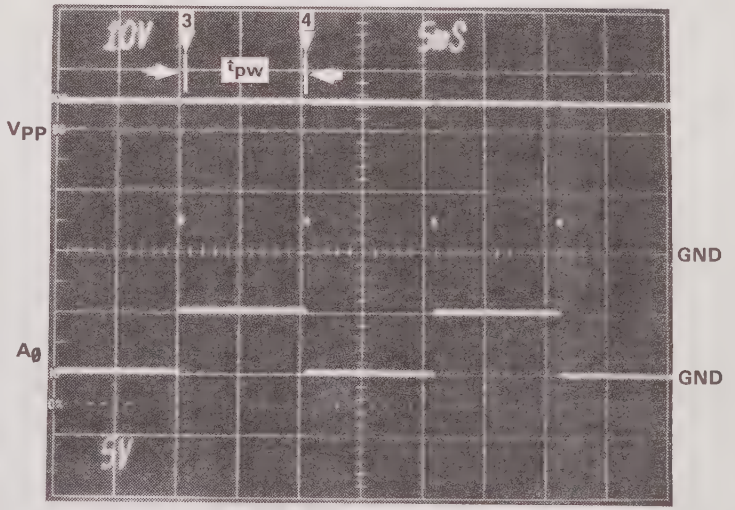
FAMILY CODES 19, 1A

DATA I/O

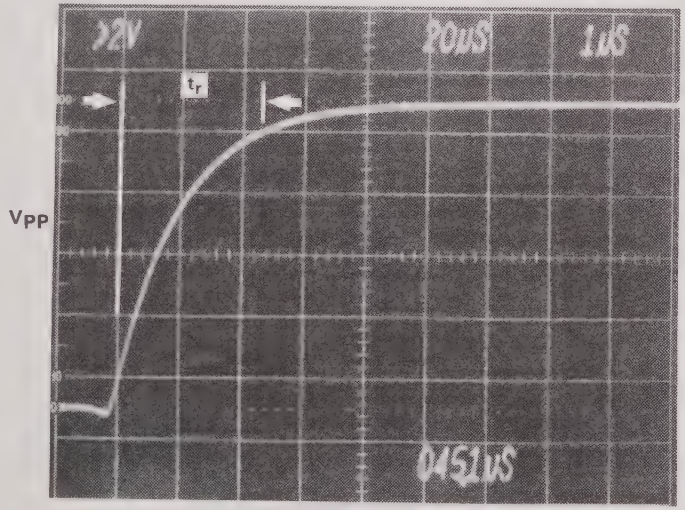
0526/1282



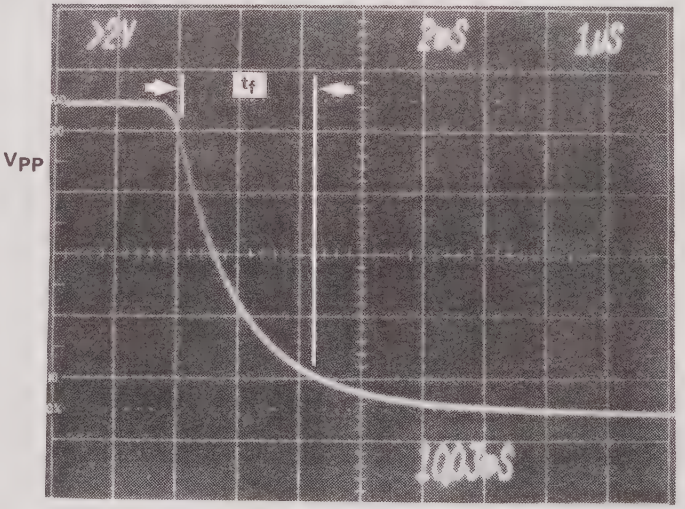
Program
1



2



3



4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	See note 3
	t_r (V_{PP})	0.5		4.0	µsec	10% - 90%
	t_f (V_{PP})	0.5		4.0	µsec	10% - 90%
	CP_1		V_{IH}		V	See note 2
	CP_2		V_{IL}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	1.9		2.1	msec	
	Pulse Count	1		20		Per byte
	Overprogram t_{pw}	9.6		10.4	msec	
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{CC}.*

Overprogram

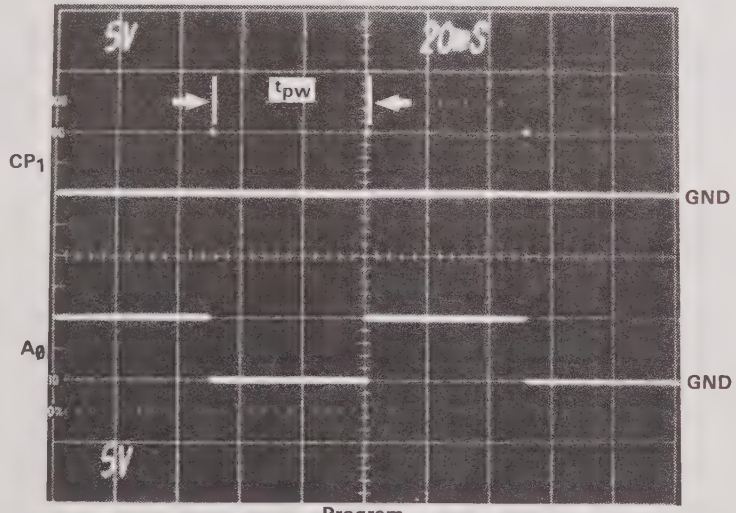
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/12/83

TIMING DIAGRAM

FAMILY CODES 25, 26

DATA I/O


5V
20mS
t_{pw}
CP_1
GND
A_0
GND
5V
Program
1

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.5	21.0	21.5	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	48		52	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*

REVISIONS

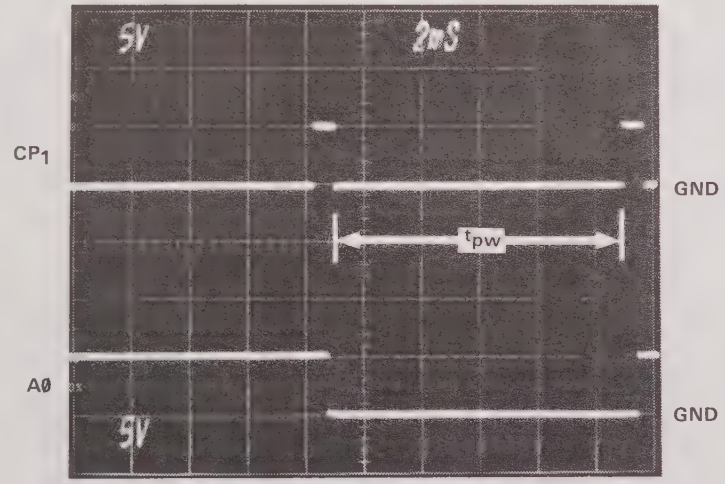
LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/08/83

TIMING DIAGRAM

FAMILY CODES 27, 28

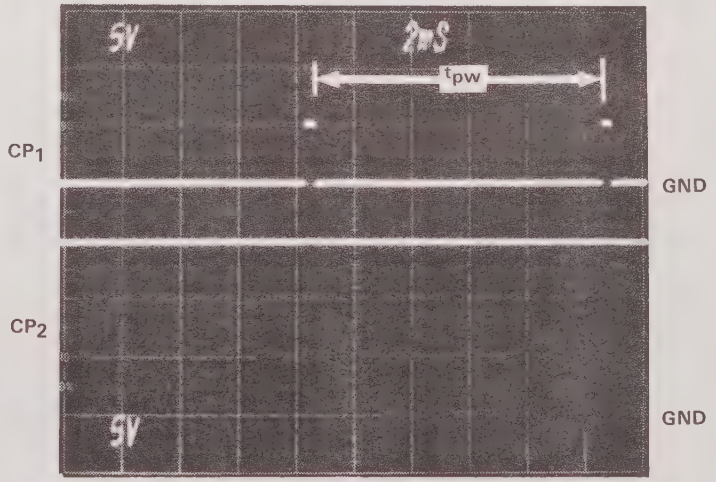
DATA I/O

0526/1282



PROGRAM

1



ERASE

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.5	21.0	21.5	V	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	9.6		10.4	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	N.A.
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CHH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.5	21.0	21.5	V	
	t_{pw}	9.6		10.4	msec	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IHH}		V	See note 5
	CP_3		V_{IL}		V	See note 2

NOTES

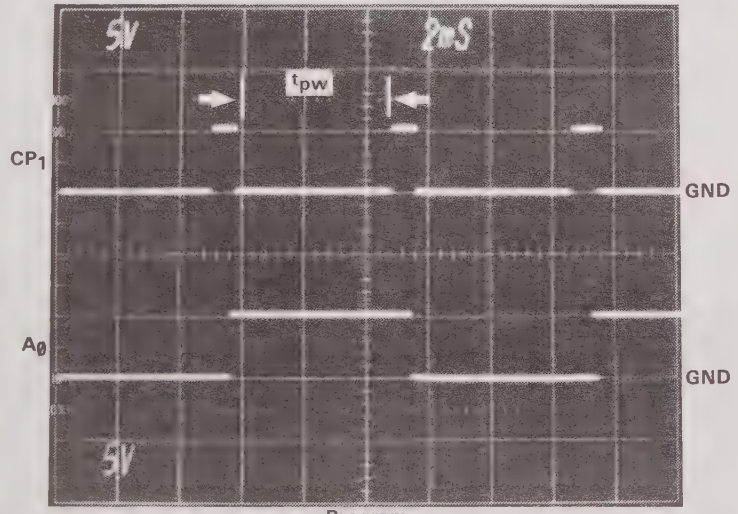
1. *Programming waveform photographs taken using calibration step 32, pinout 5A. Erase waveform photographs taken using calibration step 33, pinout 5A.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{PP} takes precedence over CP_n (Where: n = 1, 2, 3, or 4) in program and erase when they share the same pin.*
5. *V_{IHH} = Minimum 14.0 VDC.*
   = Nominal 14.5 VDC.
   = Maximum 15.0 VDC.

REVISIONS

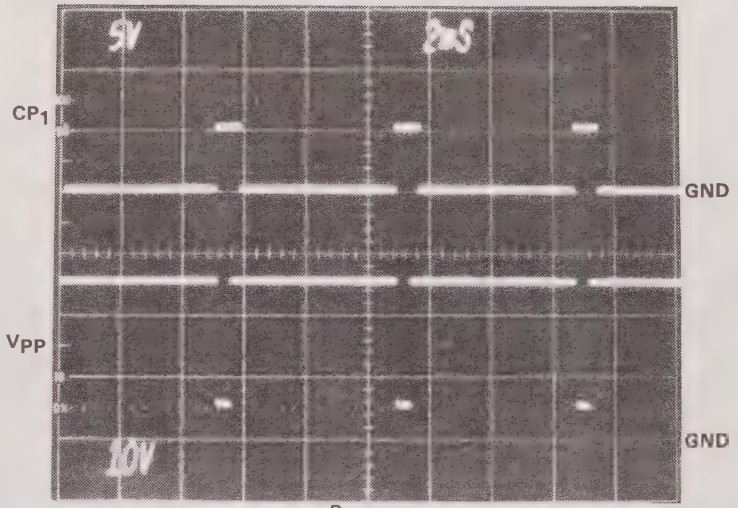
LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM
FAMILY CODES 2D, 2E

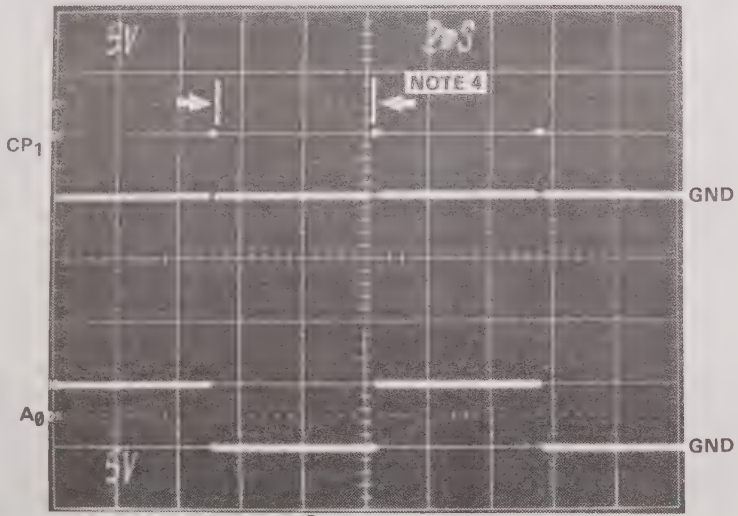
DATA I/O



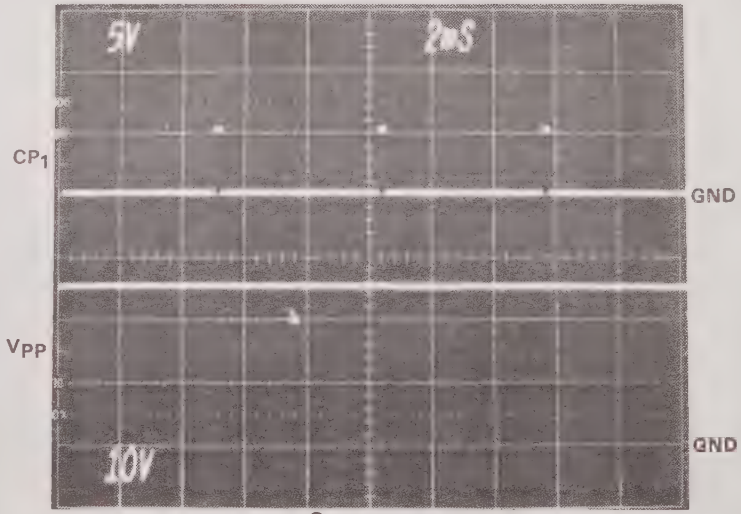
Program
1



Program
2



Overprogram
3



Overprogram
4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IL}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	4.8		5.2	msec	
	Pulse Count		5			Per byte
	Overprogram t_{pw}	4.8		26	msec	See note 4
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}				V	
ERASE	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *The length of the overprogram pulse will vary proportionally with the worst case number of pulses applied to any one byte. (This pulse is then applied to all bytes.)*

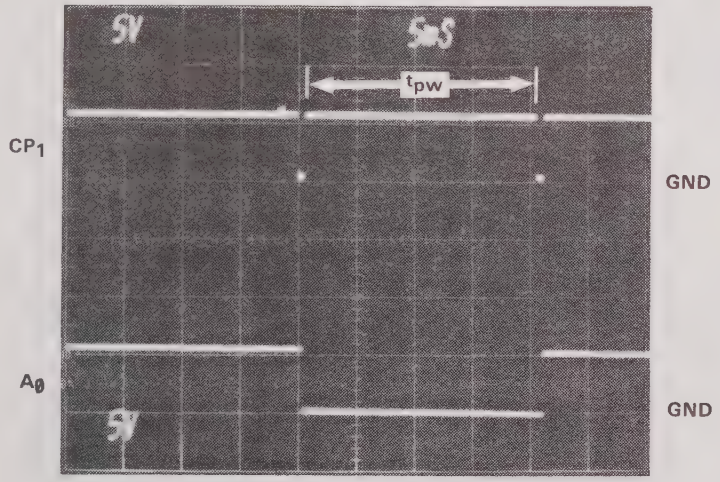
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DJ	5/18/83

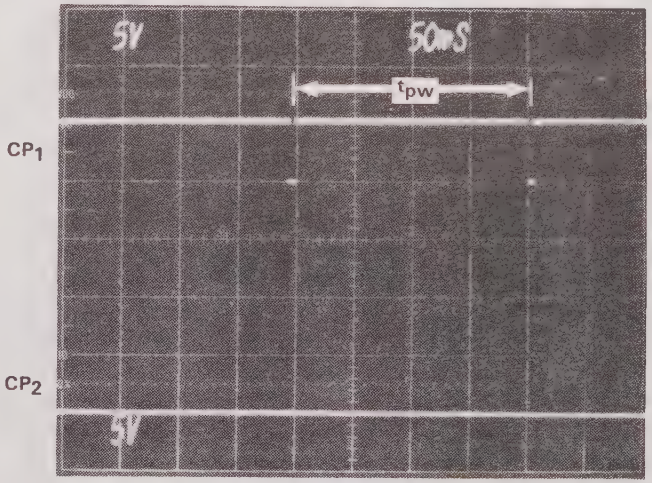
TIMING DIAGRAM

FAMILY CODES 31, 32

DATA I/O



Program
1



Erase
2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IH}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	19.0		21.0	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}	4.75	5.0	5.25	V	
ERASE	V_{PP}	24.0	25.0	26.0	V	
	t_{pw}	190		210	msec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IH}		V	See notes 2 & 3
	CP_2		V_{IL}		V	See note 2
	CP_3		V_{IL}		V	See note 2

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IL}.*

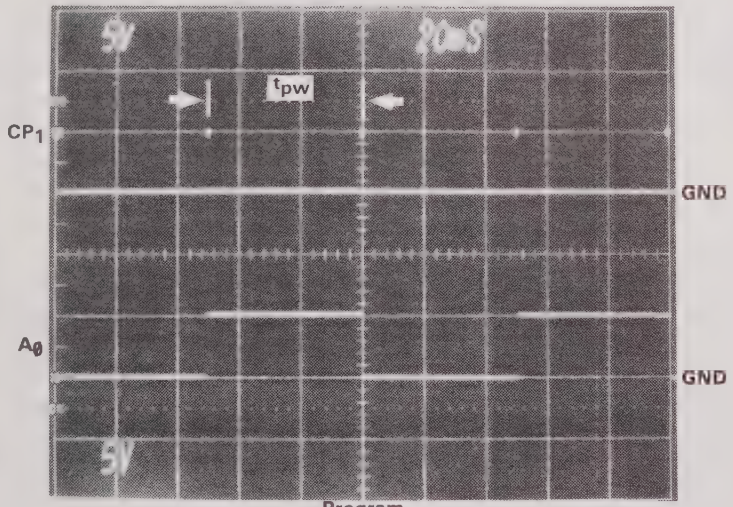
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/19/83
	ECN# 4926	DGjr	9/26/83

TIMING DIAGRAM

FAMILY CODES 33, 34

DATA I/O


5V
20mS
tpw
CP1
GND
Aø
GND
5V
Program
1

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.5	21.0	21.5	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	48		52	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	
	t_f (V_{PP})				µsec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*

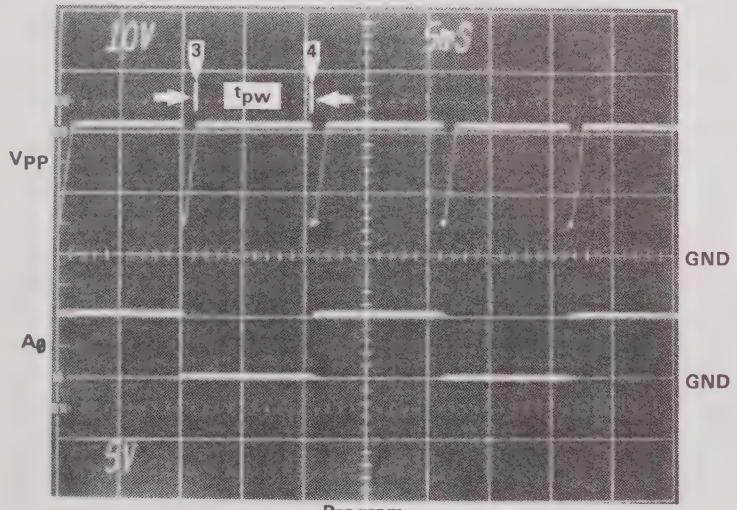
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DJ	5/18/83

TIMING DIAGRAM

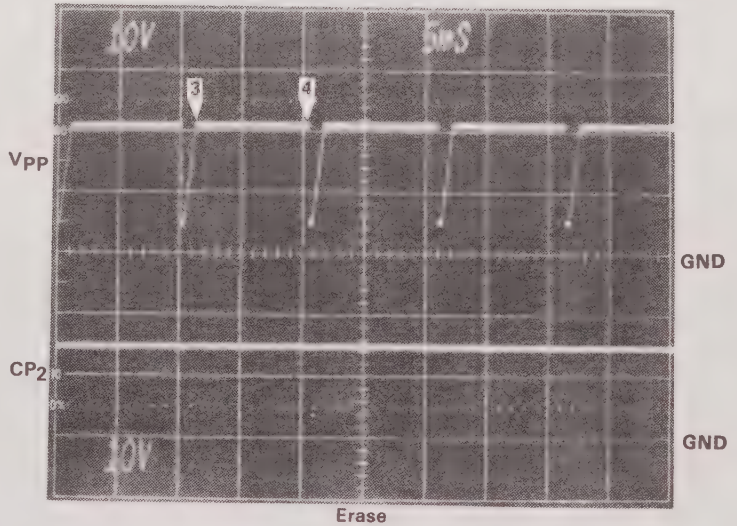
FAMILY CODES 35, 36

DATA I/O



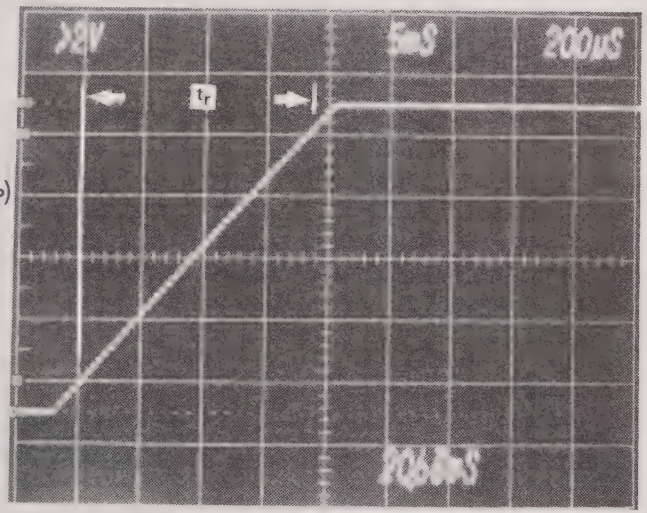
Program

1

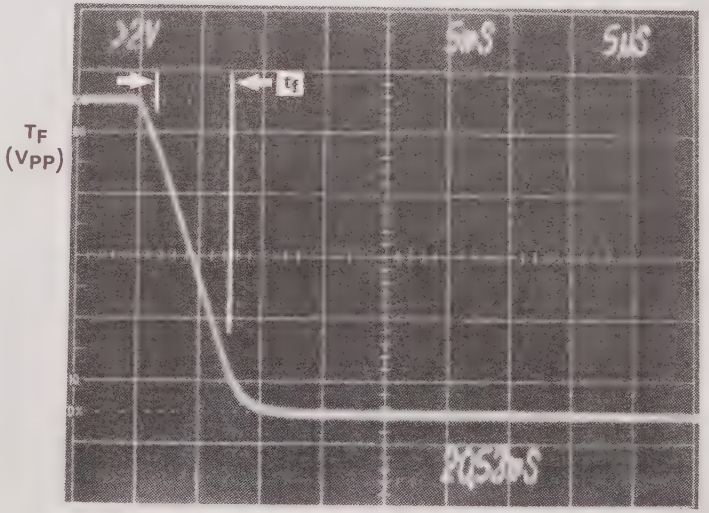


Erase

2



3



4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.0	21.0	22.0	V	See note 4
	t_r (V_{PP})	710		730	µsec	10% - 90%
	t_f (V_{PP})			100	µsec	10% - 90%
	CP_1		V_{IL}		V	See note 2
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	8.8		9.6	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.0	21.0	22.0	V	See note 4
	t_{pw}	8.8		9.6	msec	
	t_r (V_{PP})	710		730	µsec	10% - 90%
	t_f (V_{PP})			100	µsec	10% - 90%
	CP_1		V_{IL}		V	See note 2
	CP_2		V_{IHH}		V	See note 3
	CP_3		V_{IL}		V	See note 2

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *V_{IHH} = minimum 14.0 VDC.*
   = nominal 14.5 VDC.
   = maximum 15.0 VDC.
4. *Pulsed from V_{CC}.*

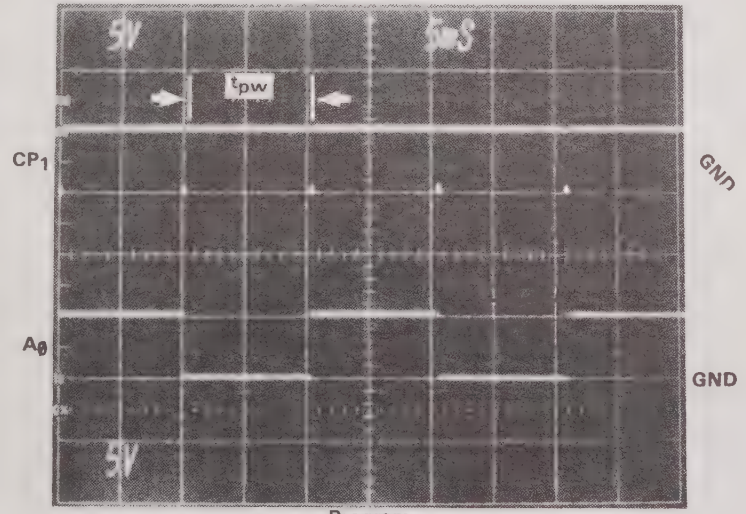
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	[illegible]	5/22/83

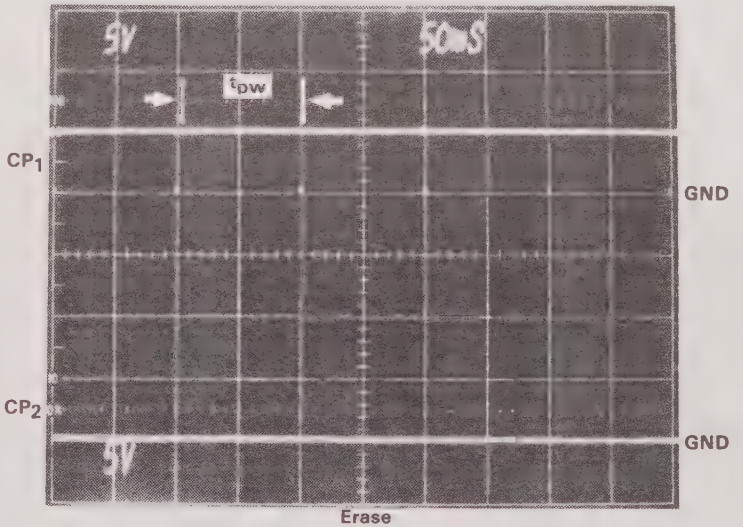
TIMING DIAGRAM

FAMILY CODES 37, 38

DATA I/O



Program
1



Erase
2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IH}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	9.6		10.4	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	
	t_{pw}	96		104	msec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IH}		V	See notes 2 & 3
	CP_2		V_{IL}		V	See note 2
	CP_3		V_{IL}		V	See note 2

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IL}.*

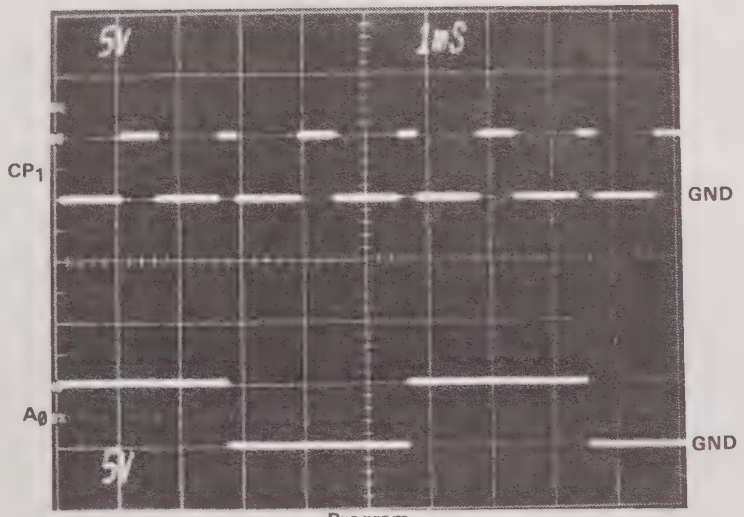
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DJ	5/18/83

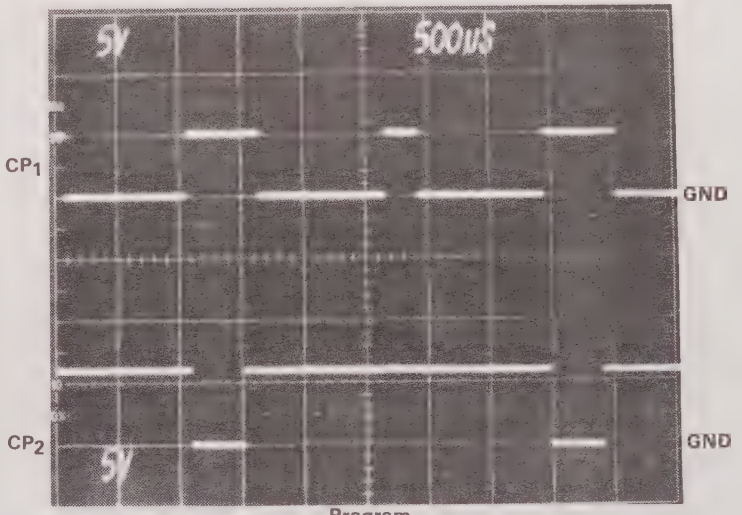
TIMING DIAGRAM

FAMILY CODES 43, 44

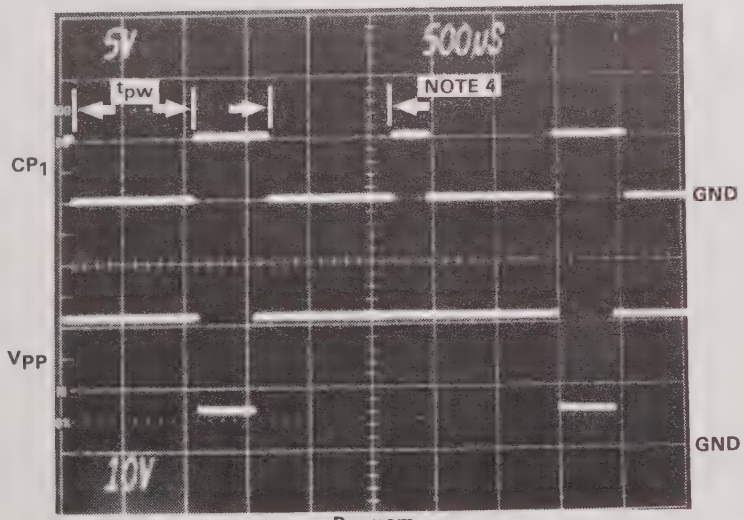
DATA I/O



Program
1



Program
2



Program
3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	5.75	6.0	6.25	V	
	V_{PP}	20.5	21.0	21.5	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.95		1.05	msec	
	Pulse Count	1		20		Per byte
	Overprogram t_{pw}	0.95		21	msec	See note 4
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}				V	
ERASE	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	
	t_f (V_{PP})				µsec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *The length of the overprogram pulse will vary proportionally with the number of pulses applied (determined and applied on a per byte basis).*

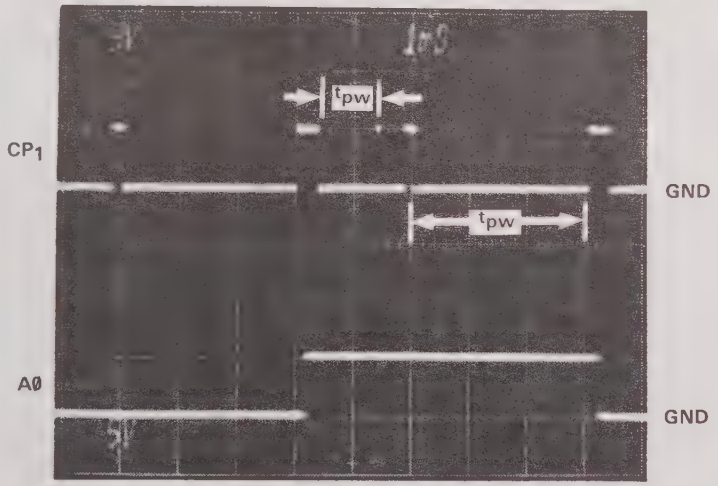
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/19/83

TIMING DIAGRAM

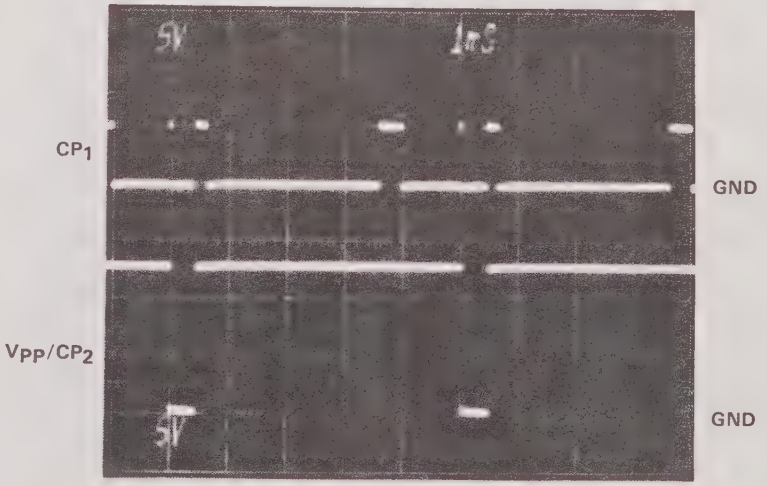
FAMILY CODES 45, 46

DATA I/O



PROGRAM

1



PROGRAM

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	5.75	6.0	6.25	V	
	V_{PP}	12.2	12.5	12.8	V	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.95		1.05	msec	
	Pulse Count	1		25		Per byte
	Overprogram t_{pw}	2.85		78.75	msec	See note 5
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CHH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}				V	
ERASE	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				usec	
	t_f (V_{PP})				usec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

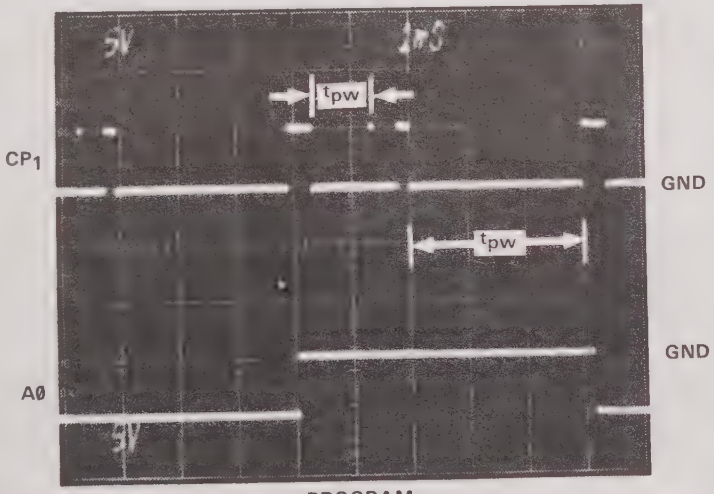
1. *Programming waveform photographs taken using calibration step 32, pinout A4.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{PP} takes precedence over CP_n (Where: n = 1, 2, 3, or 4) in program when they share the same pin.*
5. *The length of the overprogram pulse will vary proportionally with the number of pulses applied (determined and applied on a per byte basis).*

REVISIONS

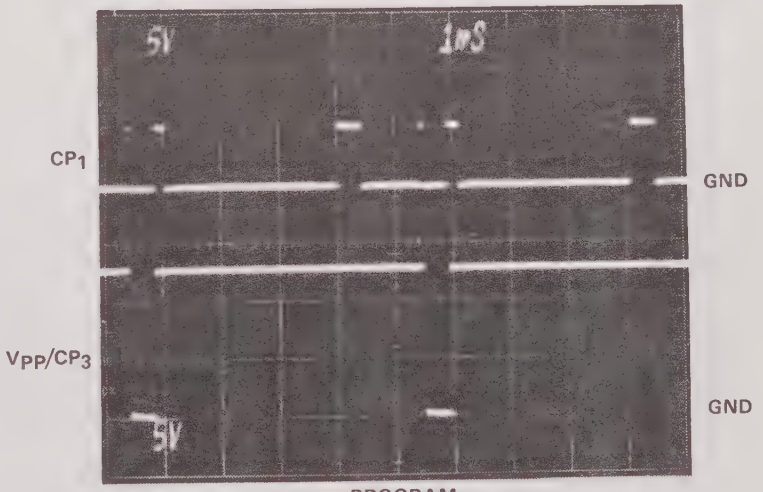
LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM
FAMILY CODES 4B, 4C

DATA I/O


5V
1mS
t_{pw}
CP_1
GND
t_{pw}
GND
A0
5V
PROGRAM

1


5V
1mS
CP_1
GND
V_{PP}/CP_3
GND
5V
PROGRAM

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	5.75	6.0	6.25	V	
	V_{PP}	12.2	12.5	12.8	V	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.95		1.05	msec	
	Pulse Count	1		25		Per byte
	Overprogram t_{pw}	2.85		78.75	msec	See note 5
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CHH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}				V	
ERASE	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				usec	
	t_f (V_{PP})				usec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 5E.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.

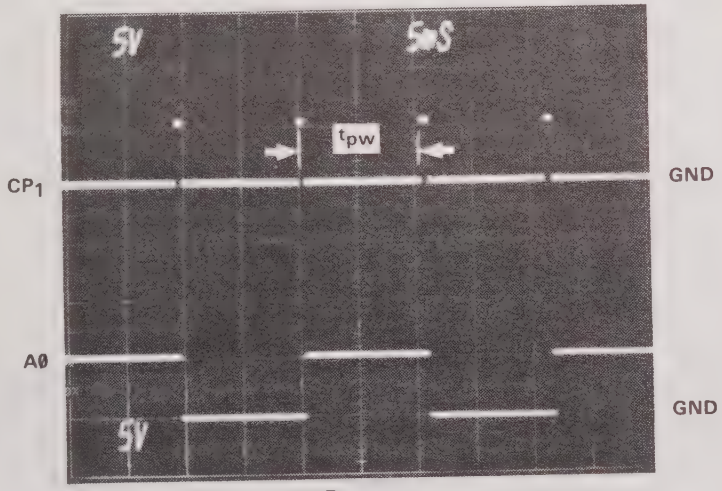
   V_{IL} = minimum −0.1 VDC.
   − maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{PP} takes precedence over CP_n (Where: n = 1, 2, 3, or 4) in program when they share the same pin.*
5. *The length of the overprogram pulse will vary proportionally with the number of pulses applied (determined and applied on a per byte basis).*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE

TIMING DIAGRAM
FAMILY CODES 5B, 5C

DATA I/O



Program
1

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.5	21.0	21.5	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	9.5		10.5	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}				V	
ERASE	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	
	t_f (V_{PP})				µsec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*

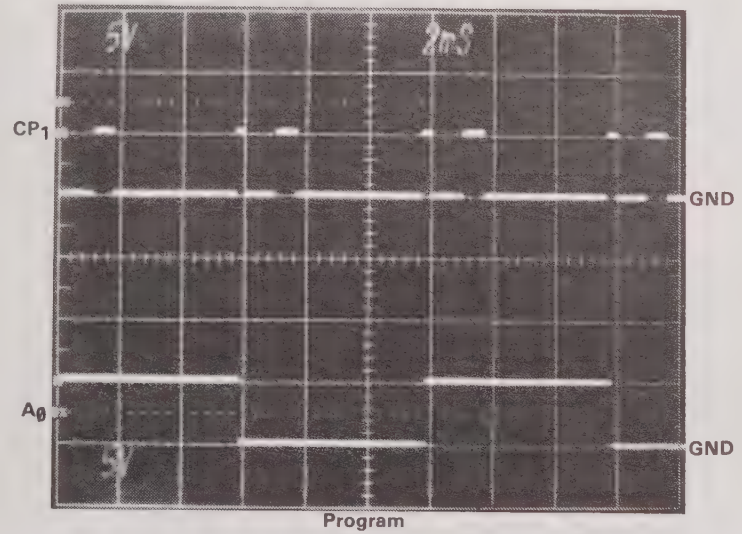
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN# 4926	Dyff	9/26/83

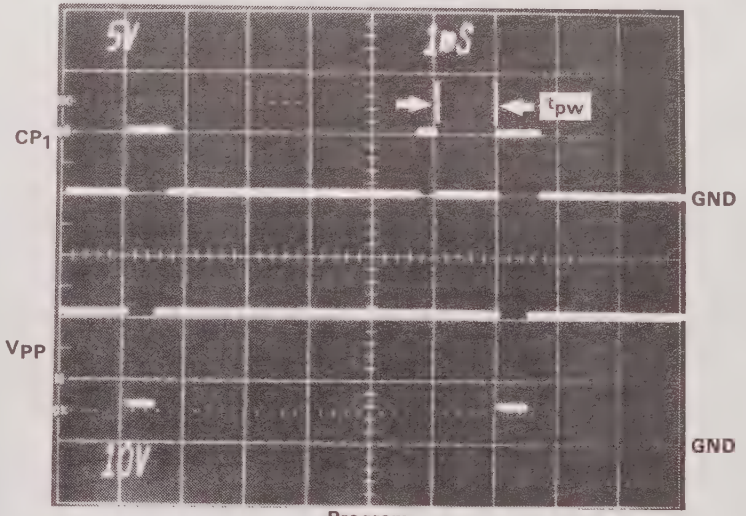
TIMING DIAGRAM

FAMILY CODES 63, 64

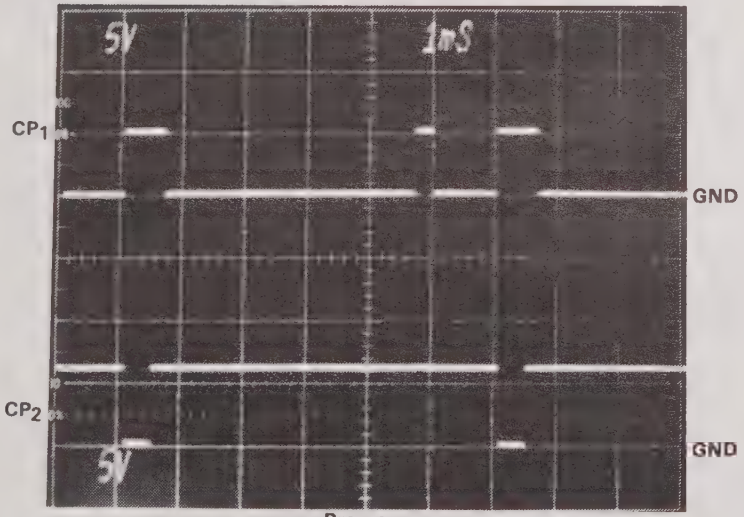
DATA I/O



Program
1



Program
2



Program
3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	5.75	6.0	6.25	V	
	V_{PP}	20.5	21.0	21.5	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.95		1.05	msec	
	Pulse Count	1		15		Per byte
	Overprogram t_{pw}	3.8		63	msec	See note 4
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	
	t_f (V_{PP})				µsec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *The length of the overprogram pulse will vary proportionally with the number of pulses applied (determined and applied on a per byte basis).*

REVISIONS

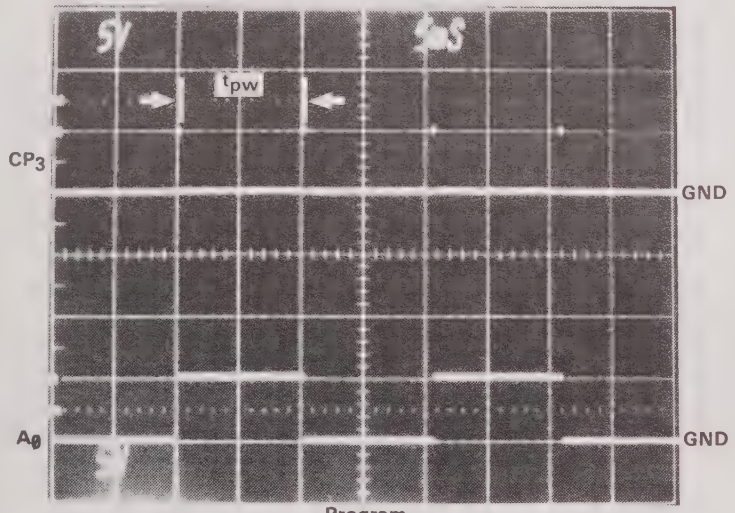
LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/13/83

TIMING DIAGRAM

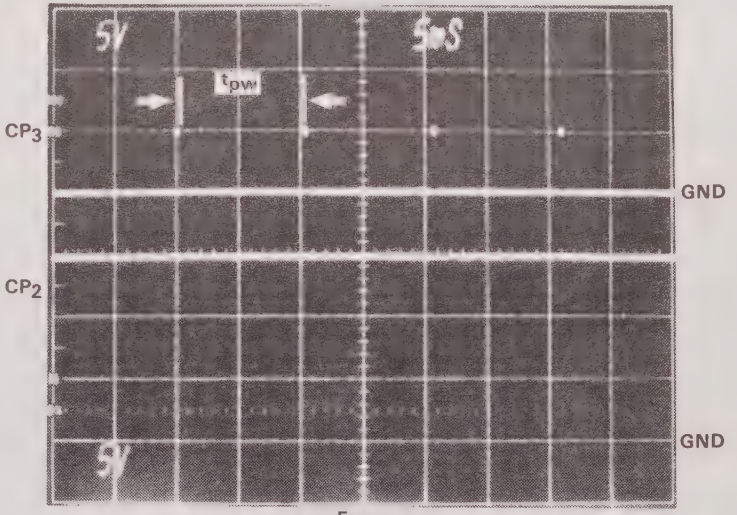
FAMILY CODES 79, 7A

DATA I/O

0526/1282



Program
1



Erase
2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.0	21.0	22.0	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See note 2
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See notes 2 & 3
	t_{pw}	9.6		10.4	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}	4.75	5.0	5.25	V	
ERASE	V_{PP}	20.0	21.0	22.0	V	
	t_{pw}	9.6		10.4	msec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See note 2
	CP_2		V_{IHH}		V	See note 4
	CP_3		V_{IL}		V	See note 2 & 3

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{IHH} = minimum 14.0 VDC.*
   = nominal 14.5 VDC.
   = maximum 15.0 VDC.

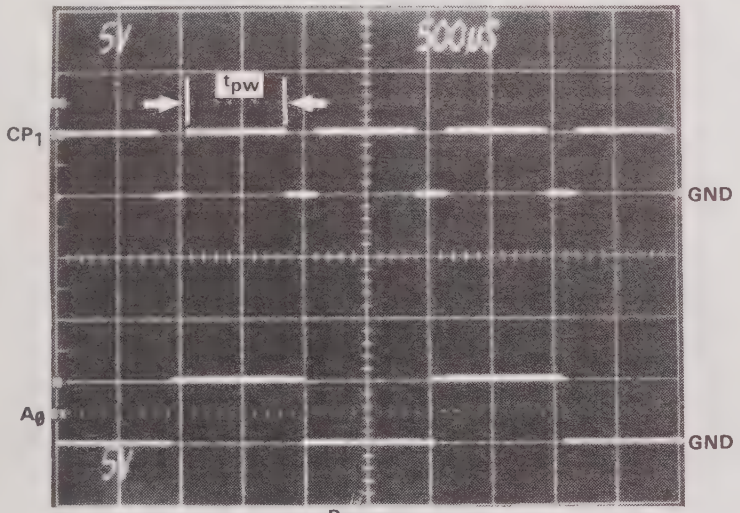
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/19/83

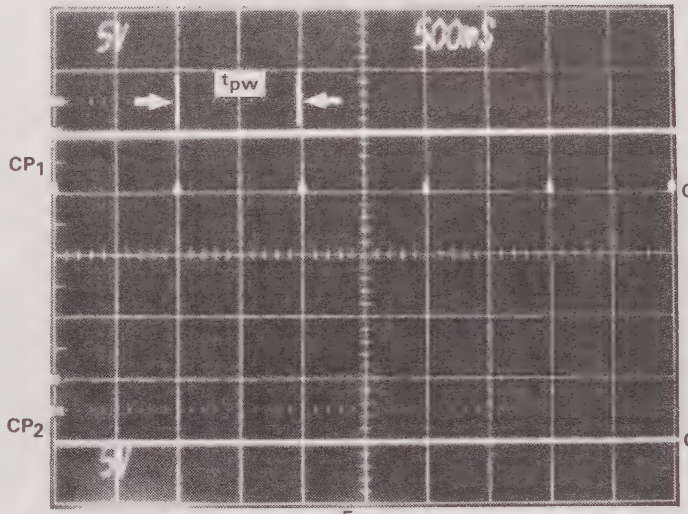
TIMING DIAGRAM

FAMILY CODES 81, 82

DATA I/O



Program
1



Erase
2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IH}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.8		1.0	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	
	t_{pw}	.96		1.04	sec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IH}		V	See notes 2 & 3
	CP_2		V_{IL}		V	See note 2
	CP_3		V_{IL}		V	See note 2

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IL}.*

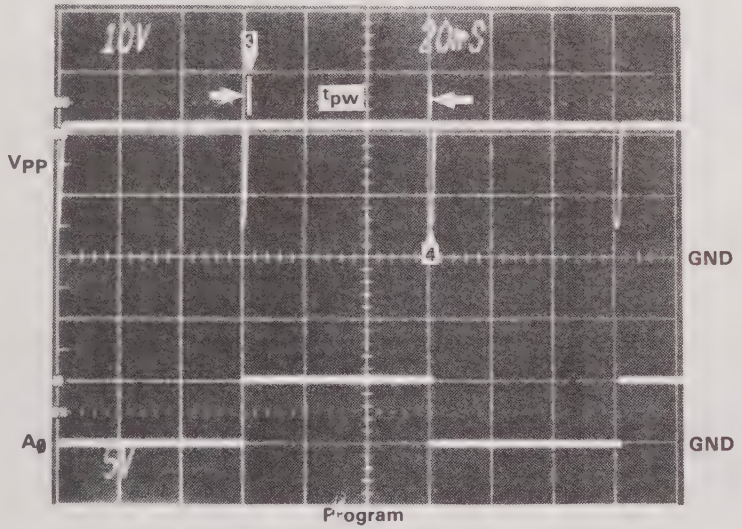
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DM	5/18/83

TIMING DIAGRAM

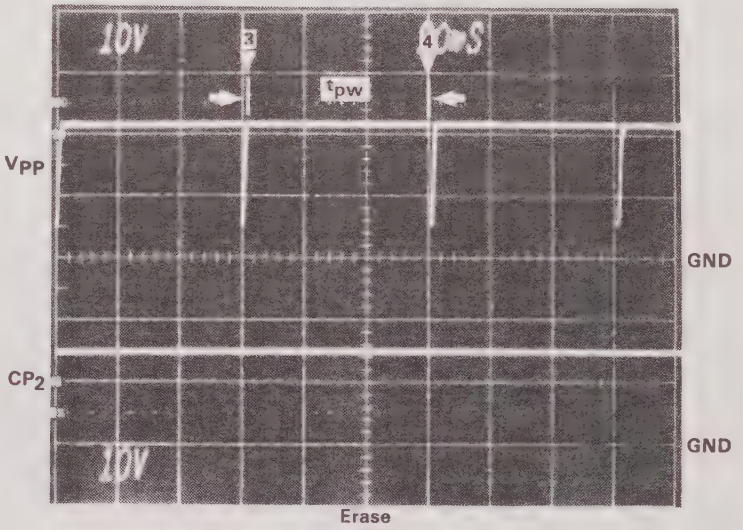
FAMILY CODES 83, 84

DATA I/O



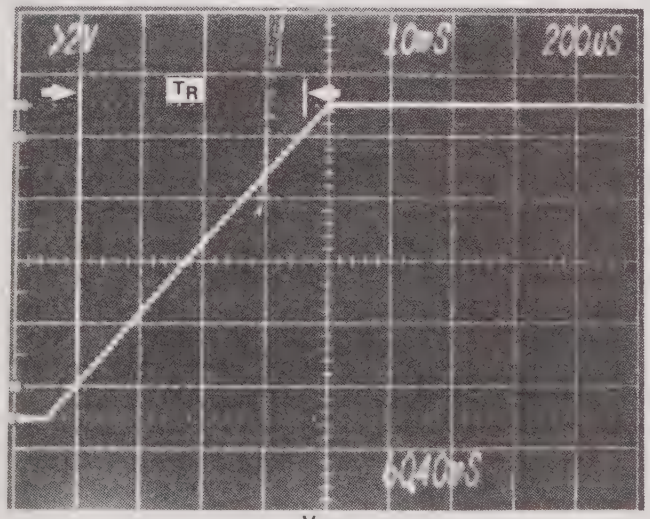
Program

1



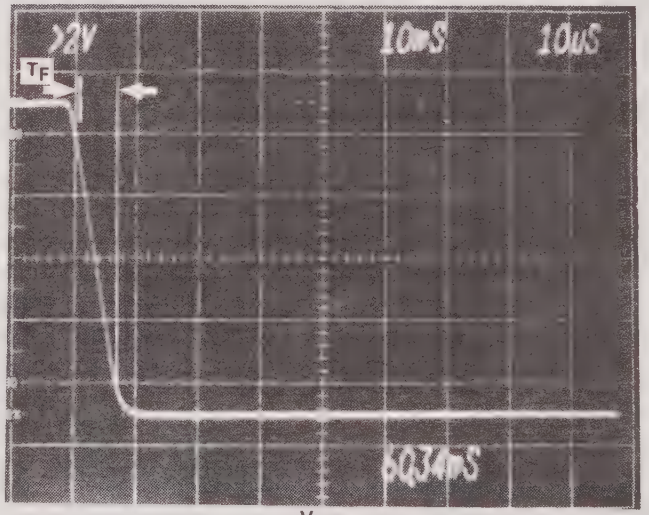
Erase

2



VPP

3



VPP

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.0	21.0	22.0	V	See note 3
	t_r (V_{PP})	710		730	µsec	10% - 90%
	t_f (V_{PP})			100	µsec	10% - 90%
	CP_1		V_{IL}		V	See note 2
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	57		63	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.0	21.0	22.0	V	See note 3
	t_{pw}	57		63	msec	
	t_r (V_{PP})	710		730	µsec	10% - 90%
	t_f (V_{PP})			100	µsec	10% - 90%
	CP_1		V_{IL}		V	See note 2
	CP_2		V_{IHH}		V	See note 4
	CP_3		V_{IL}		V	See note 2

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{CC}.*
4. *V_{IHH} = minimum 14.0 VDC.*
   = nominal 14.5 VDC.
   = maximum 15.0 VDC.

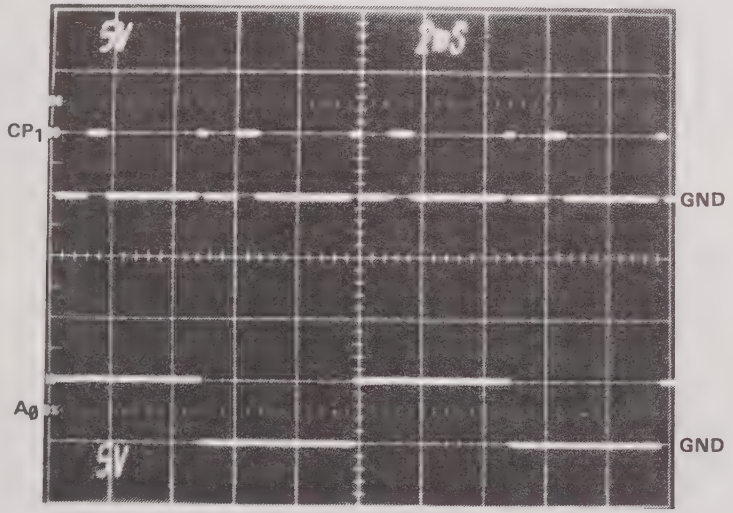
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release		5-29-85

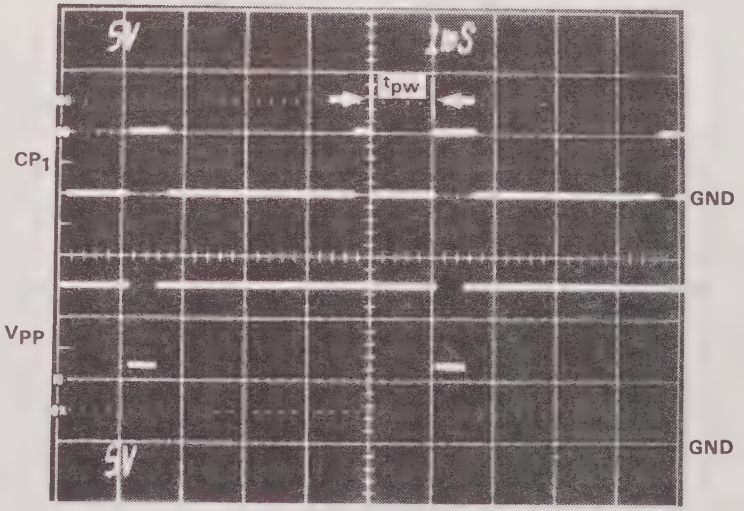
TIMING DIAGRAM

FAMILY CODES 85, 86

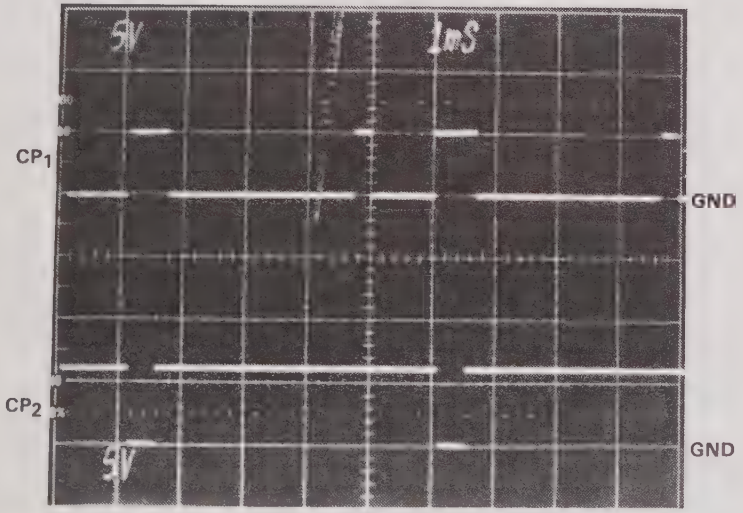
DATA I/O


5V
2mS
CP1
GND
A0
GND
5V

1


5V
1mS
tpw
CP1
GND
VPP
GND
5V

2


5V
1mS
CP1
GND
CP2
GND
5V

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	5.75	6.0	6.25	V	
	V_{PP}	12.2	12.5	12.8	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.95		1.05	msec	
	Pulse Count	1		25		Per byte
	Overprogram t_{pw}	2.85		78.75	msec	See note 4
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	
	t_f (V_{PP})				µsec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *The length of the overprogram pulse will vary proportionally with the number of pulses applied (determined and applied on a per byte basis).*

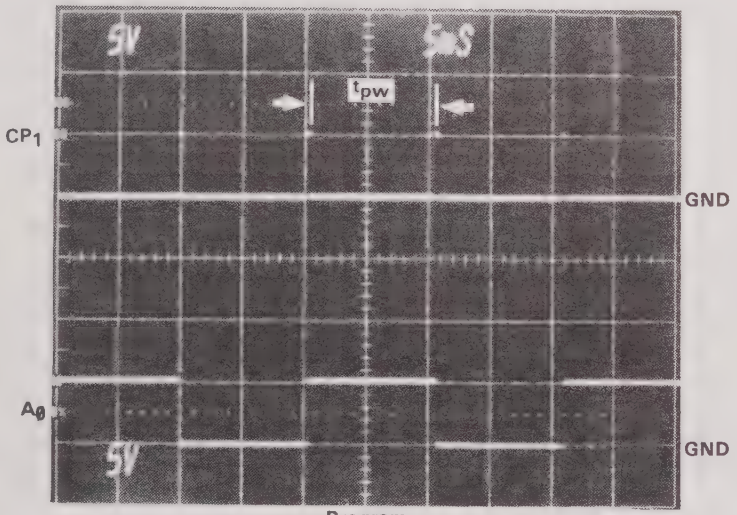
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/18/93

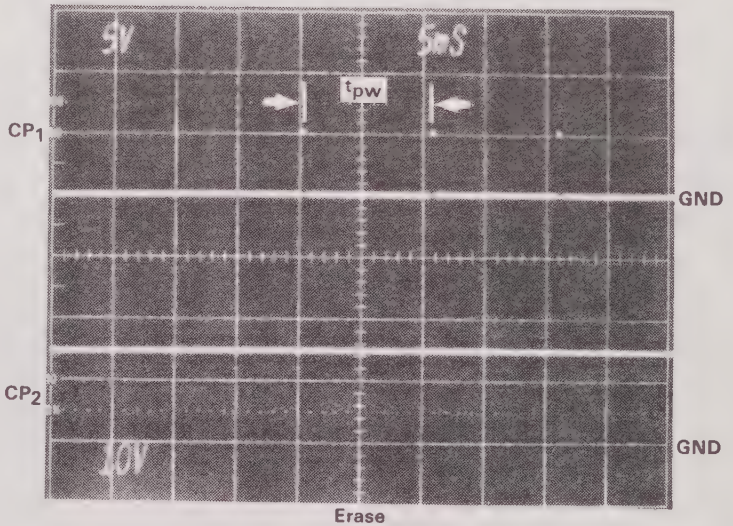
TIMING DIAGRAM

FAMILY CODES 93, 94

DATA I/O



Program
1



Erase
2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	-0.1	0	0.8	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	9.6		10.4	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	-0.1	0	0.8	V	
	t_{pw}	9.6		10.4	msec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IHH}		V	See note 4
	CP_3		V_{IL}		V	See note 2

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}*
4. *V_{IHH} = minimum 14.0 VDC.*
   = nominal 14.5 VDC.
   = maximum 15.0 VDC.

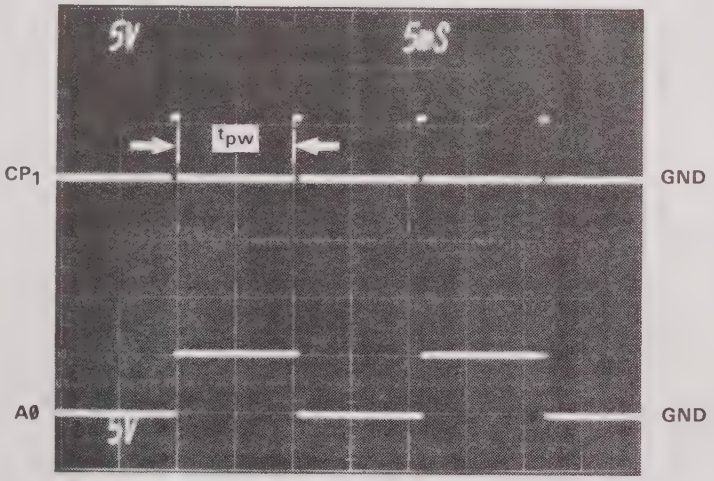
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	BY	5/18/83
	ECN# 4926	BWP	9/26/83

TIMING DIAGRAM

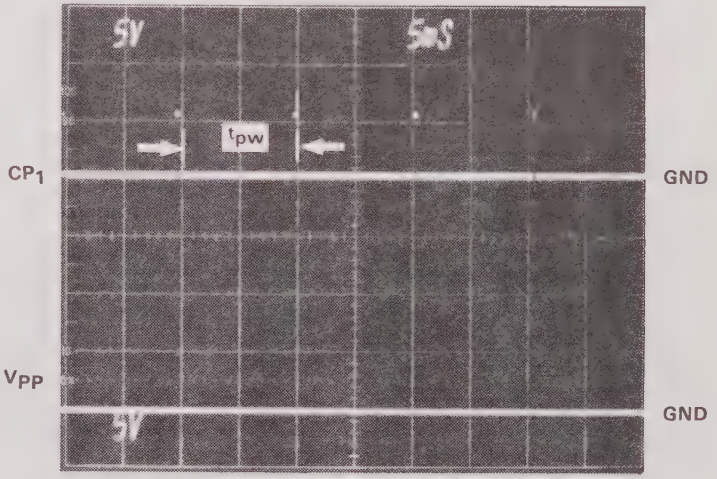
FAMILY CODES A5, A6

DATA I/O



Program

1



Erase

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	4.75	5.0	5.25	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	9.5		10.5	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	-0.1	0	0.8	V	
	t_{pw}	9.5		10.5	sec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*

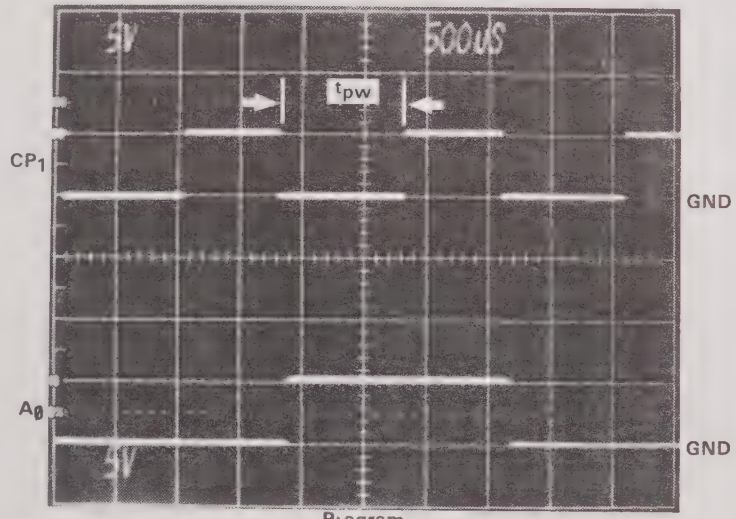
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN# 4926		9/26/83

TIMING DIAGRAM

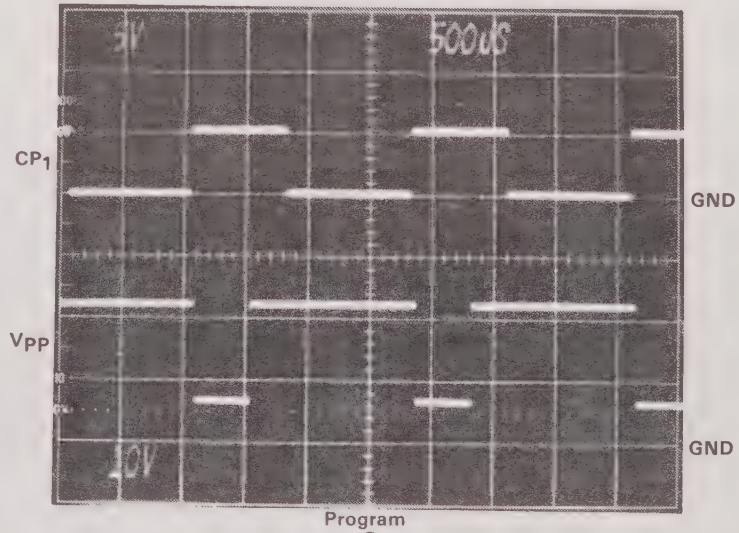
FAMILY CODES AB, AC

DATA I/O



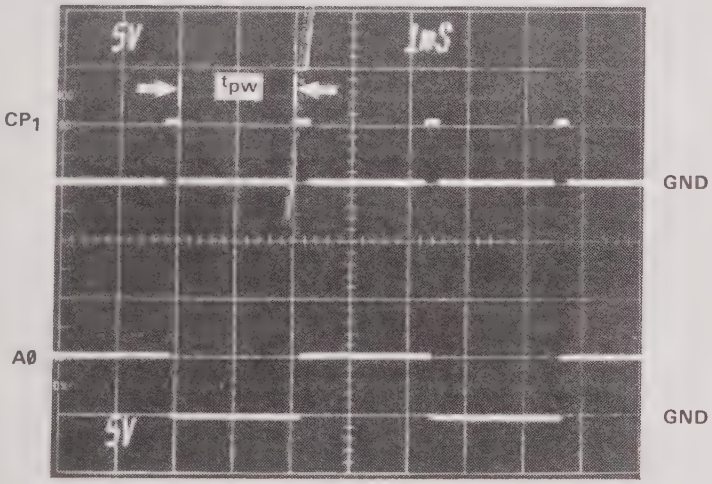
Program

1



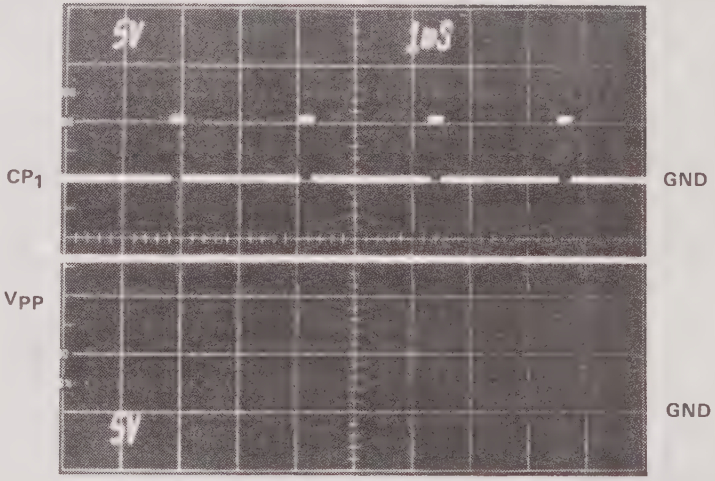
Program

2



Overprogram

3



Overprogram

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	5.75	6.0	6.25	V	
	V_{PP}	21.0	21.5	22.0	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.95		1.05	msec	
	Pulse Count	1		25		Per byte
	Overprogram t_{pw}	1.9		2.1	msec	
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.5	5.6	5.7	V	2nd pass
CHIP	V_{CC}				V	
ERASE	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	
	t_f (V_{PP})				µsec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*

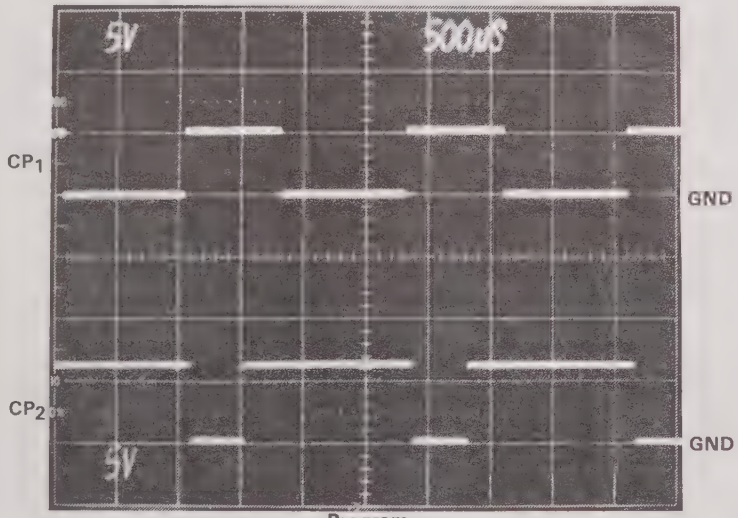
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DCF	5/10/83
	ECN# 4990	[illegible]	11/11/83

TIMING DIAGRAM

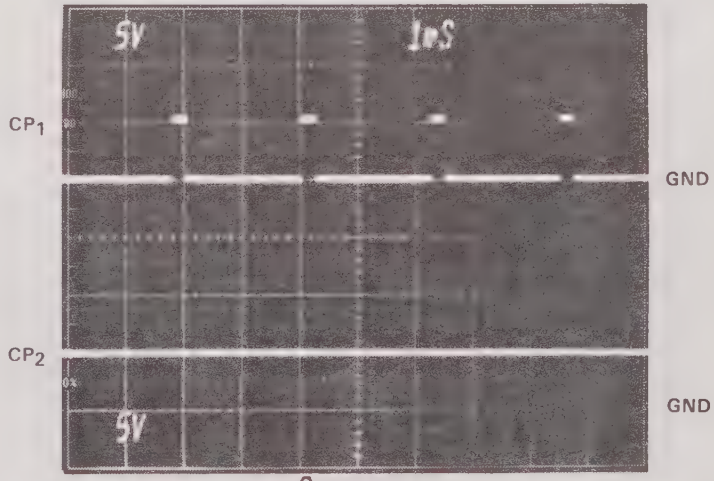
FAMILY CODES AF, B0

DATA I/O



Program

5



Overprogram

6

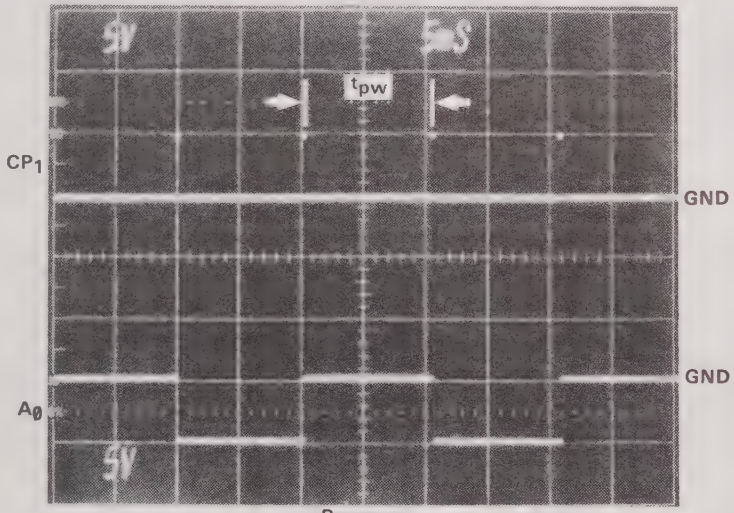
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DG	5/18/83
	ECN# 4990	DG	11/1/83

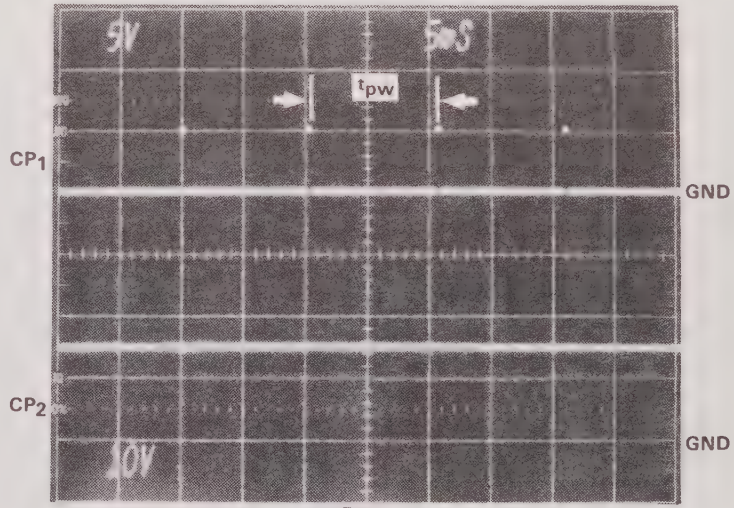
TIMING DIAGRAM

FAMILY CODES AF, B0

DATA I/O



Program
1



Erase
2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.0	21.0	22.0	V	NA
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	9.6		10.4	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	20.0	21.0	22.0	V	
	t_{pw}	9.6		10.4	msec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IHH}		V	See note 4
	CP_3		V_{IL}		V	See note 2

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{IHH} = minimum 14.0 VDC.*
   = nominal 14.5 VDC.
   = maximum 15.0 VDC.

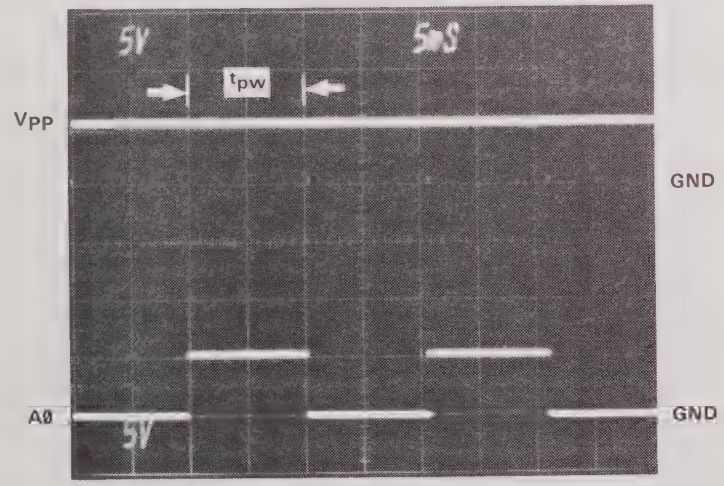
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DJ	5/24/83

TIMING DIAGRAM

FAMILY CODES B3, B4

DATA I/O


5V
5mS
tpw
VPP
GND
A0
GND
5V
PROGRAM
1

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	-0.1	0	0.8	V	See note 3
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See note 2
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	9.6		10.4	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	N.A.
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CHH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				msec	
	t_r (V_{PP})				usec	
	t_f (V_{PP})				usec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*

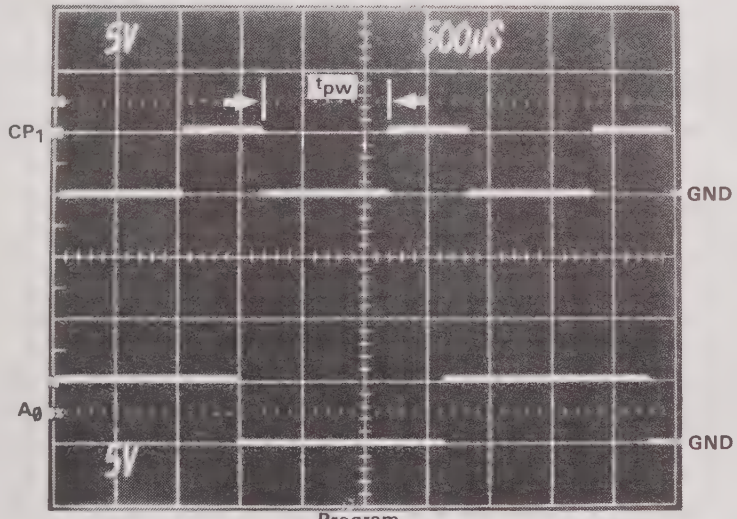
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
		MJB	4/10/85

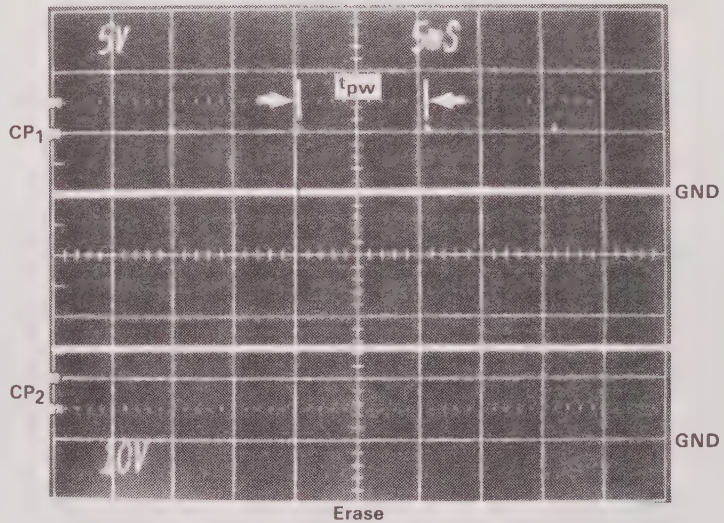
TIMING DIAGRAM

FAMILY CODES B7, B8

DATA I/O



Program
1



Erase
2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	-0.1	0	0.8	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.96		1.04	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	-0.1	0	0.8	V	
	t_{pw}	9.6		10.4	msec	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IHH}		V	See note 4
	CP_3		V_{IL}		V	See note 2

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{IHH} = minimum 14.0 VDC.*
   = nominal 14.5 VDC.
   = maximum 15.0 VDC.

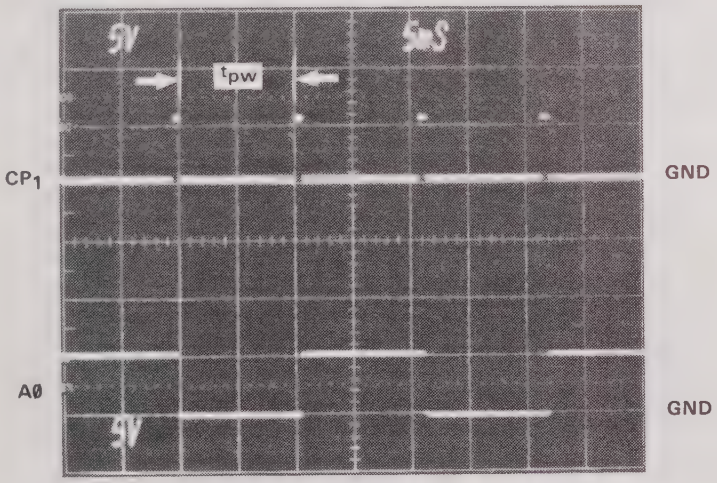
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	Release	DH	5/13/83
	ECN# 4926	DMJO	9/26/83
	ECN# 4990	MH	11/16/83

TIMING DIAGRAM

FAMILY CODES B9, BA

DATA I/O



Program
1

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	24.0	25.0	26.0	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IL}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	9.5	1	10.5	msec	
	Pulse Count					Per byte
	Overprogram t_{pw}				msec	NA
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	
	t_f (V_{PP})				µsec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*

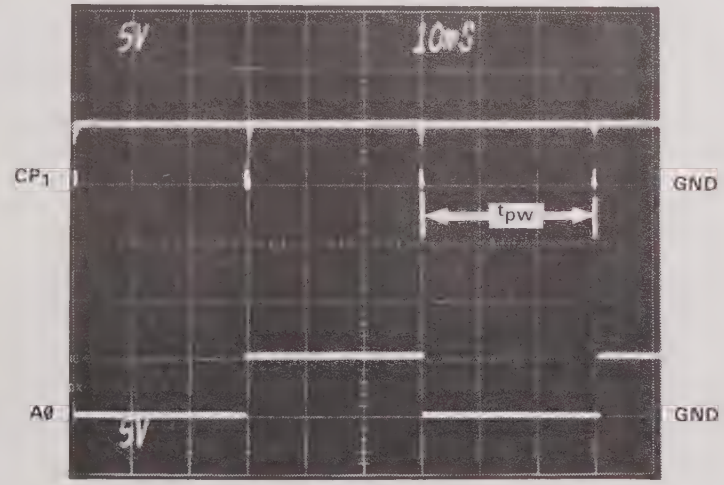
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN# 4926	Dfyp	9/26/03

TIMING DIAGRAM

FAMILY CODES BD, BE

DATA I/O



PROGRAM
1

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	-.1	0	0.8	V	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	29.0		31.0	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	N.A.
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CHH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}				V	
ERASE	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				usec	
	t_f (V_{PP})				usec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

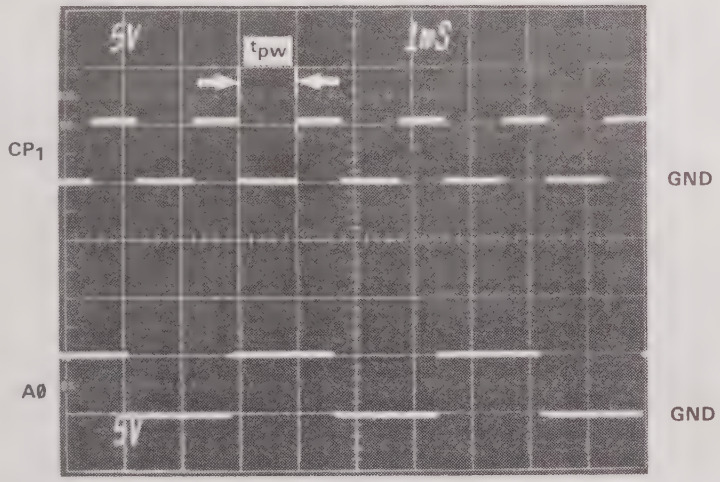
1. *Programming waveform photographs taken using calibration step 32, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*

REVISIONS

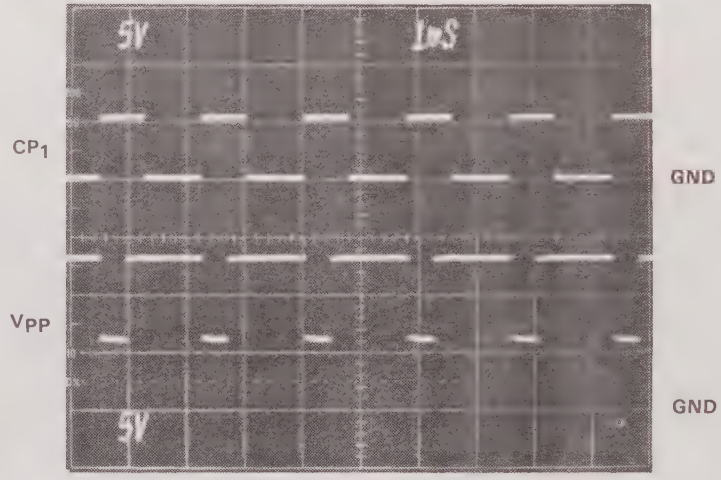
LTR	DESCRIPTION	P.E.	DATE
		MJB	1/10/85

TIMING DIAGRAM
FAMILY CODES BF, CO

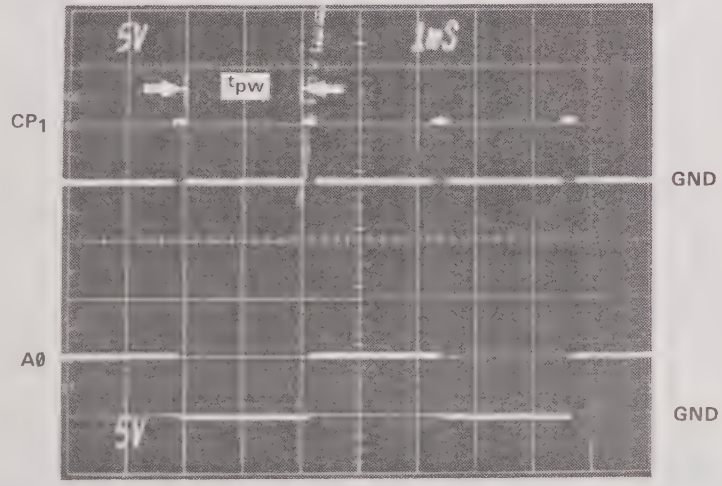
DATA I/O



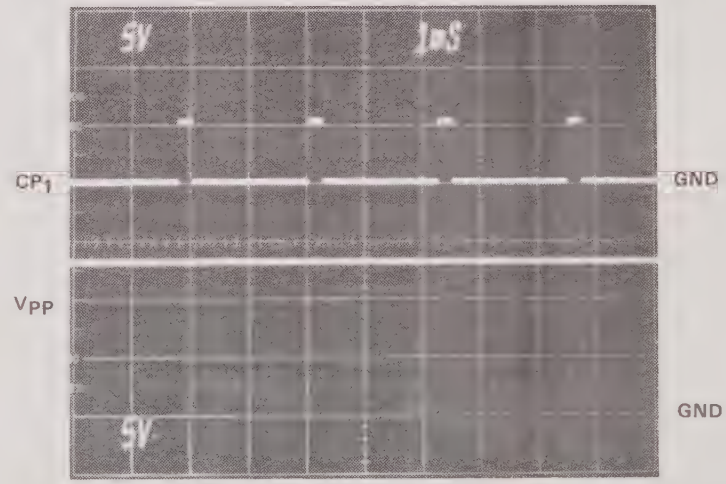
Program
1



Program
2



Overprogram
3



Overprogram
4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	5.75	6.0	6.25	V	
	V_{PP}	12.5	13.0	13.5	V	
	t_r (V_{PP})				µsec	NA
	t_f (V_{PP})				µsec	NA
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.95	1	1.05	msec	
	Pulse Count	1		25		Per byte
	Overprogram t_{pw}	1.9		2.1	msec	
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CCH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				µsec	
	t_f (V_{PP})				µsec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 33. Erase waveform photographs taken using calibration step 33, pinout 33.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*

REVISIONS

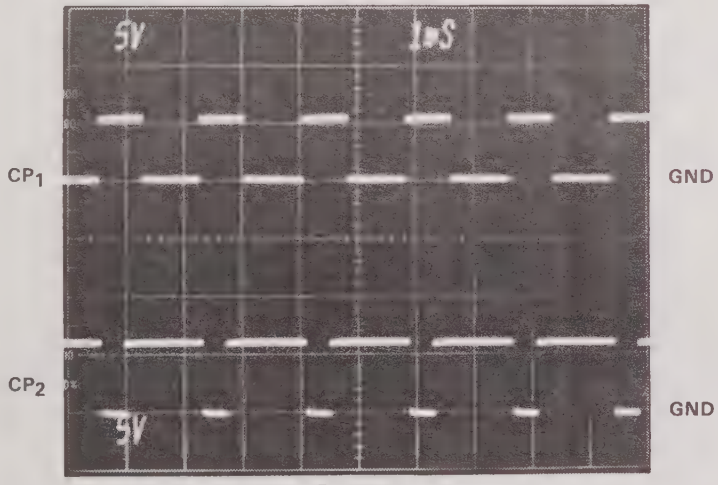
LTR	DESCRIPTION	P.E.	DATE
	ECN# 4926	Dyp	9/26/83

TIMING DIAGRAM

FAMILY CODES C1, C2

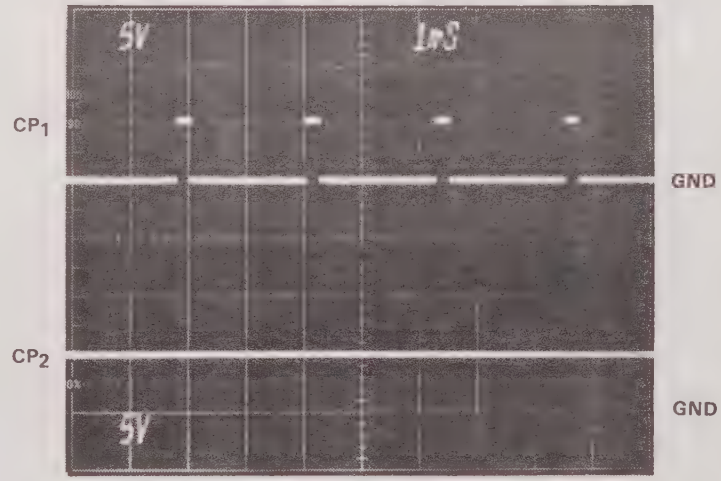
DATA I/O

0526/1282



Program

5



Overprogram

6

REVISIONS

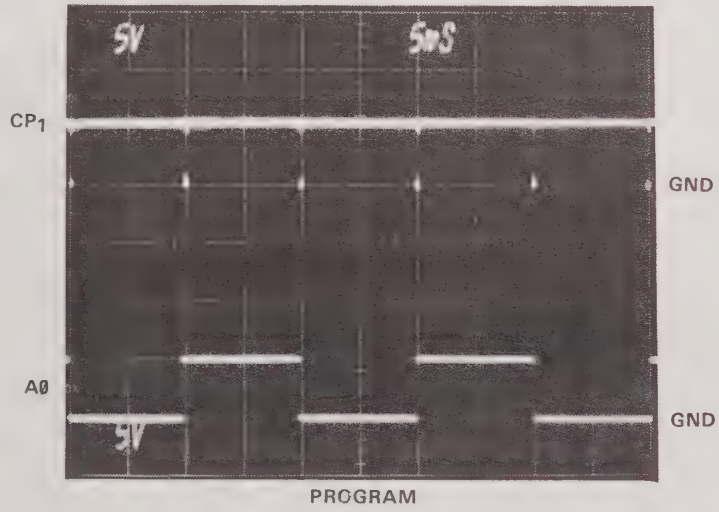
LTR	DESCRIPTION	P.E.	DATE
	ECN# 4926		

TIMING DIAGRAM

FAMILY CODES C1, C2

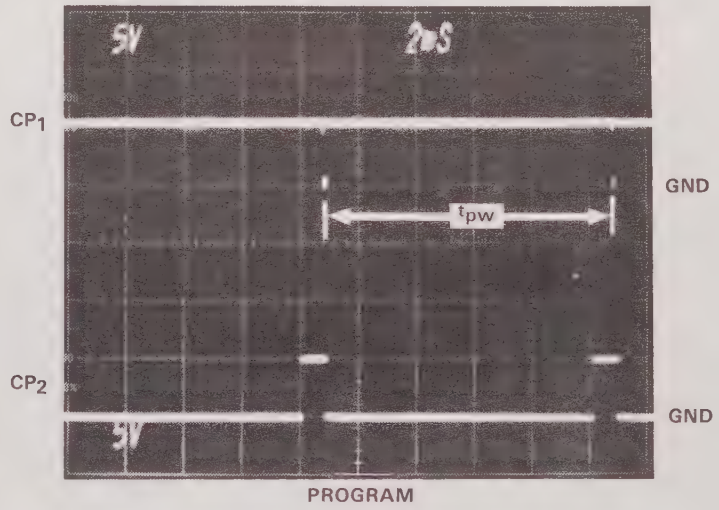
Sheet 2 of 2

DATA I/O



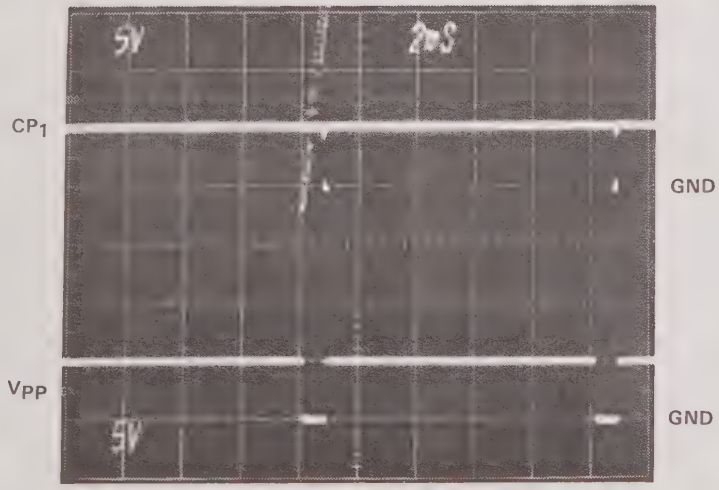
PROGRAM

1



PROGRAM

2



PROGRAM

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	-0.1	0	0.8	V	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	1.5		12.0	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	N.A.
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CHH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				msec	
	t_r (V_{PP})				usec	
	t_f (V_{PP})				usec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 98.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.

   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{PP} takes precedence over CP_n (Where: n = 1, 2, 3, or 4) in program when they share the same pin.*

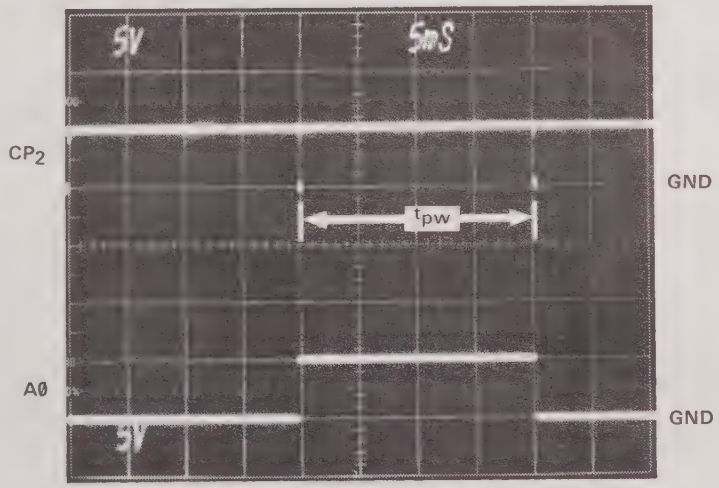
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
		NBB	1/10/85

TIMING DIAGRAM

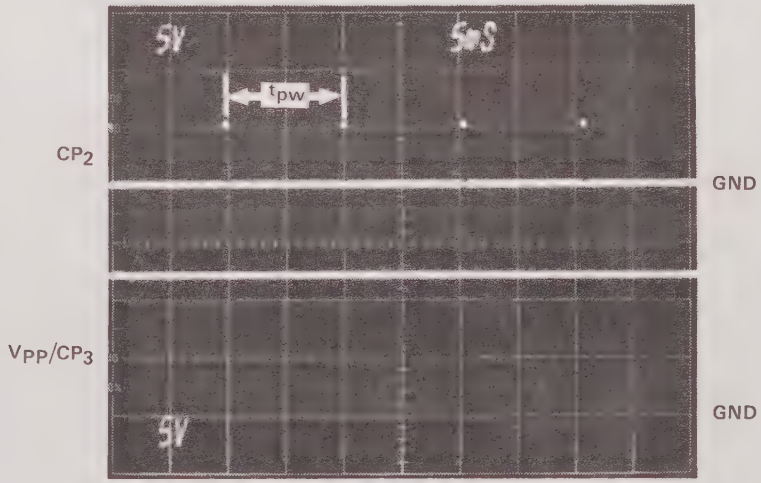
FAMILY CODES C3, C4

DATA I/O



PROGRAM

1



ERASE

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	4.75	5.0	5.25	V	
	V_{PP}	4.75	5.0	5.25	V	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See note 2
	CP_2		V_{IL}		V	See notes 2 & 3
	CP_3				V	N.A.
	t_{pw}	19.0		21.0	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	N.A.
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CHH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}	4.75	5.2	5.25	V	
ERASE	V_{PP}	11.5	12.0	12.5	V	
	t_{pw}	9.5		10.5	msec	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See note 2
	CP_2		V_{IL}		V	See notes 2 & 3
	CP_3				V	NA

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout A6. Erase waveform photographs taken using calibration step 33, pinout A6.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.

   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{PP} takes precedence over CP_n (Where: n = 1, 2, 3, or 4) in program and erase when they share the same pin.*

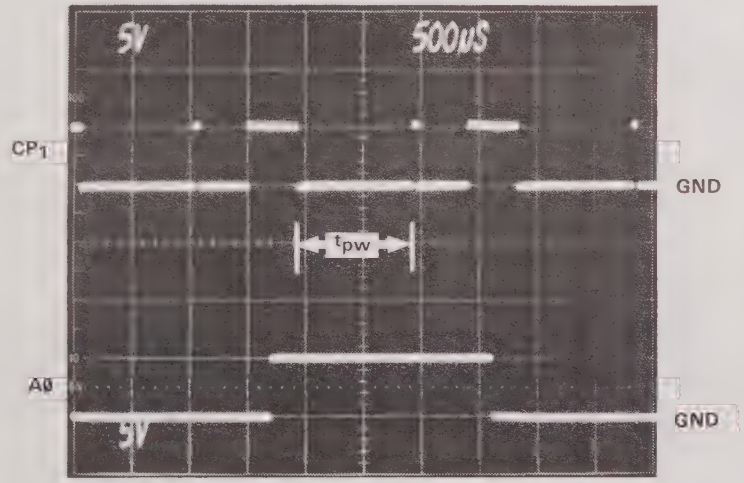
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
		[illegible]	4/10/85

TIMING DIAGRAM

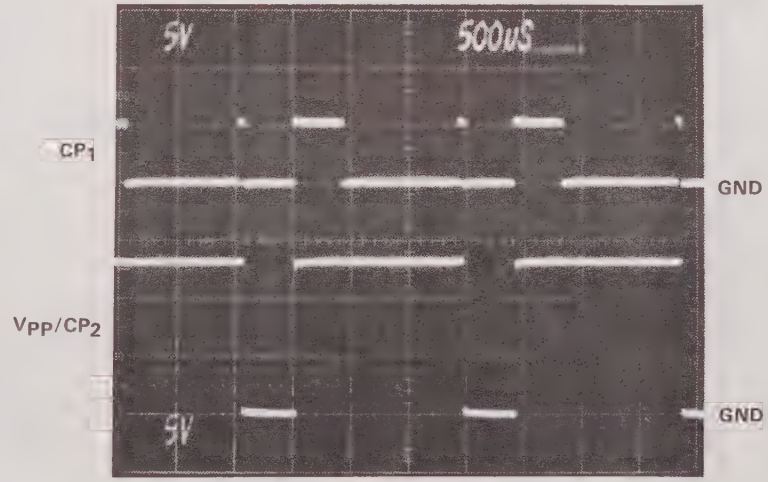
FAMILY CODES C9, CA

DATA I/O



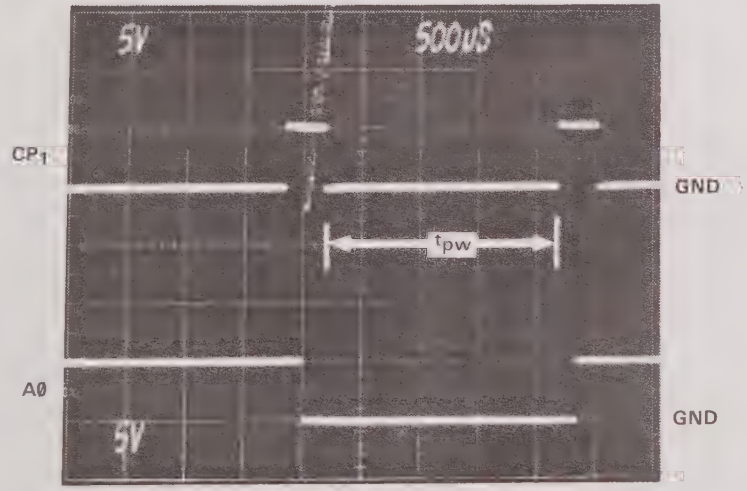
PROGRAM

1



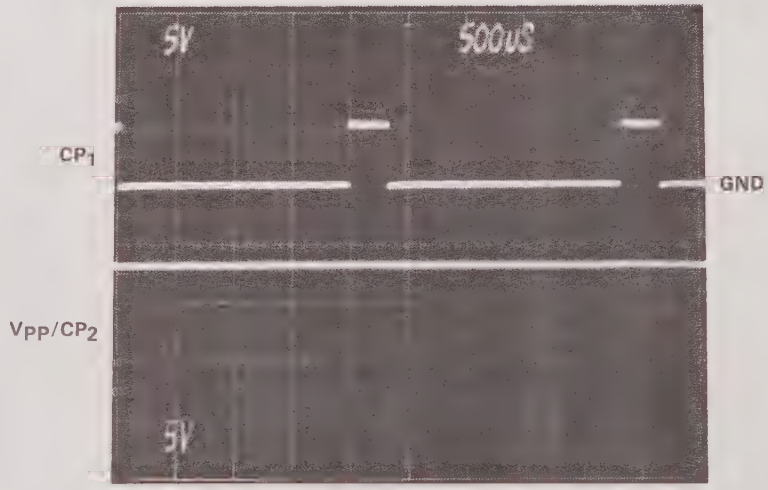
PROGRAM

2



OVERPROGRAM

3



OVERPROGRAM

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	5.75	6.0	6.25	V	
	V_{PP}	12.7	13.0	13.3	V	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3		V_{IL}		V	See note 2
	t_{pw}	0.95		1.05	msec	
	Pulse Count	1		25		Per byte
	Overprogram t_{pw}	1.9		2.1	msec	
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CHH}	5.1	5.2	5.3	V	2nd pass
CHIP	V_{CC}				V	
ERASE	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				usec	
	t_f (V_{PP})				usec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout A4.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{PP} takes precedence over CP_n (Where: n = 1, 2, 3, or 4) in program when they share the same pin.*

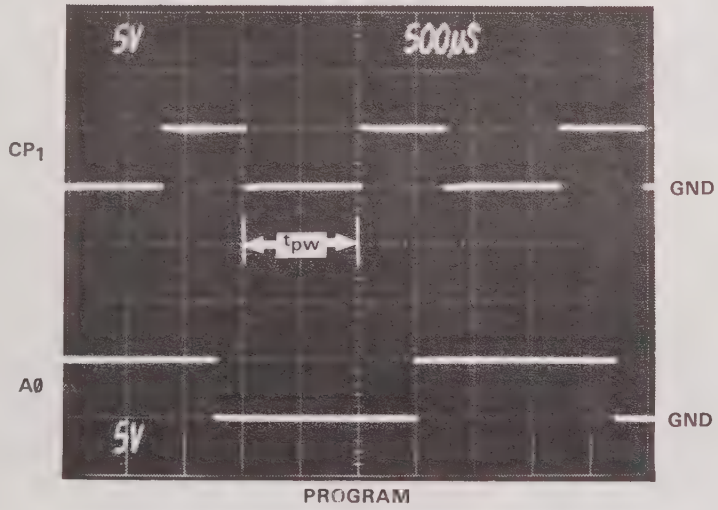
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
		9998	4/10/85

TIMING DIAGRAM

FAMILY CODES DD, DE

DATA I/O


5V
500µS
CP1
GND
tpw
A0
5V
GND
PROGRAM
1

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CC}	5.75	6.0	6.25	V	
	V_{PP}	20.5	21.0	21.5	V	
	t_r (V_{PP})				usec	N.A.
	t_f (V_{PP})				usec	N.A.
	CP_1		V_{IL}		V	See notes 2 & 3
	CP_2		V_{IH}		V	See note 2
	CP_3				V	N.A.
	t_{pw}	0.95		1.05	msec	
	Pulse Count		1			Per byte
	Overprogram t_{pw}				msec	N.A.
VERIFY	V_{CCL}	4.7	4.8	4.9	V	1st pass
	V_{CHH}	5.1	5.2	5.3	V	2nd pass
CHIP ERASE	V_{CC}				V	
	V_{PP}				V	
	t_{pw}				sec	
	t_r (V_{PP})				usec	
	t_f (V_{PP})				usec	
	CP_1				V	
	CP_2				V	
	CP_3				V	

NOTES

1. *Programming waveform photographs taken using calibration step 32, pinout 32.*
2. *V_{IH} = minimum 2.2 VDC.*
   = maximum V_{CC} + 0.5 VDC.
   V_{IL} = minimum −0.1 VDC.
   = maximum 0.8 VDC.
3. *Pulsed from V_{IH}.*
4. *V_{PP} takes precedence over CP_n (Where: n = 1, 2, 3, or 4) in program when they share the same pin.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
		[illegible]83	1/13/85

TIMING DIAGRAM

FAMILY CODES F7, F8

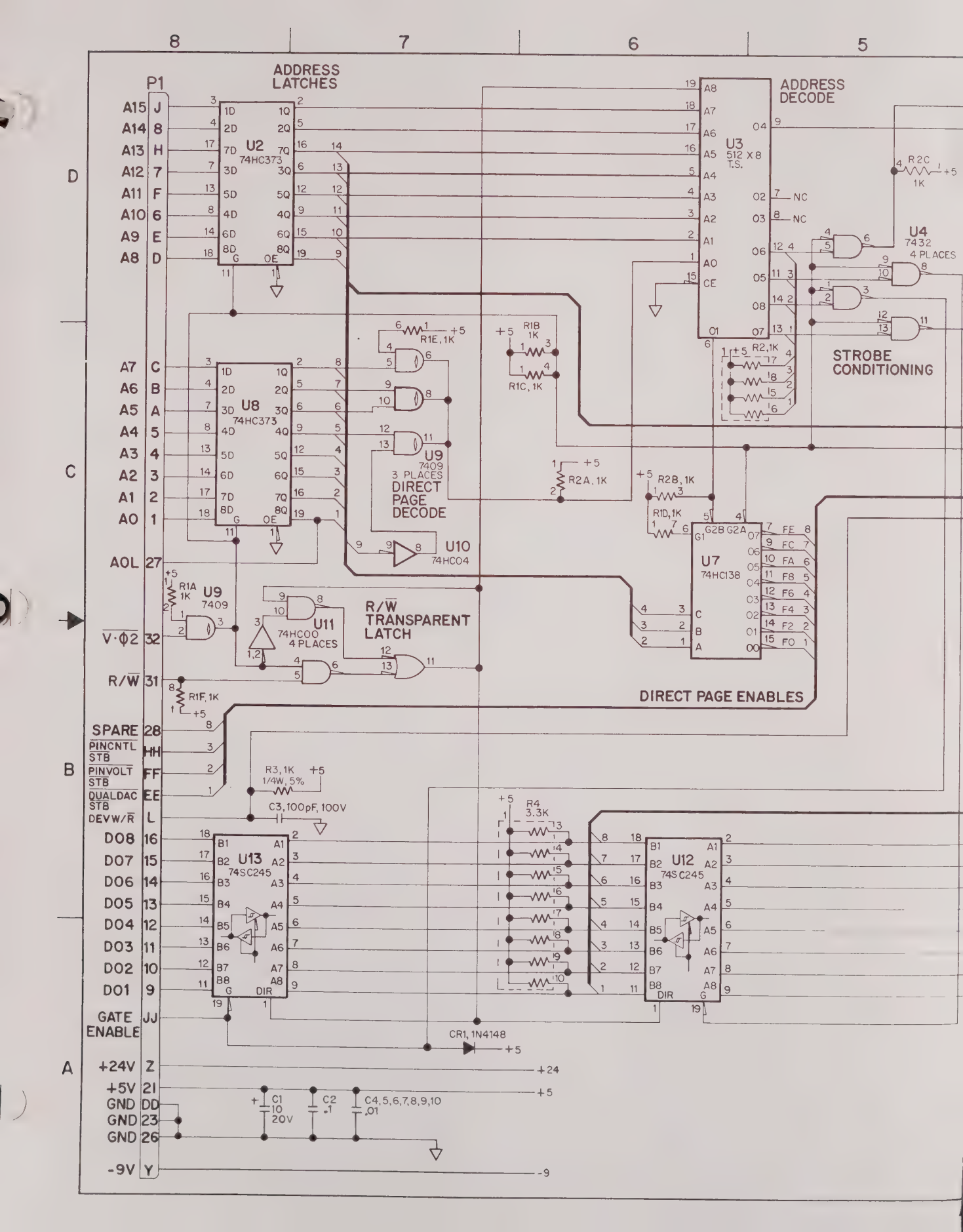
DATA I/O

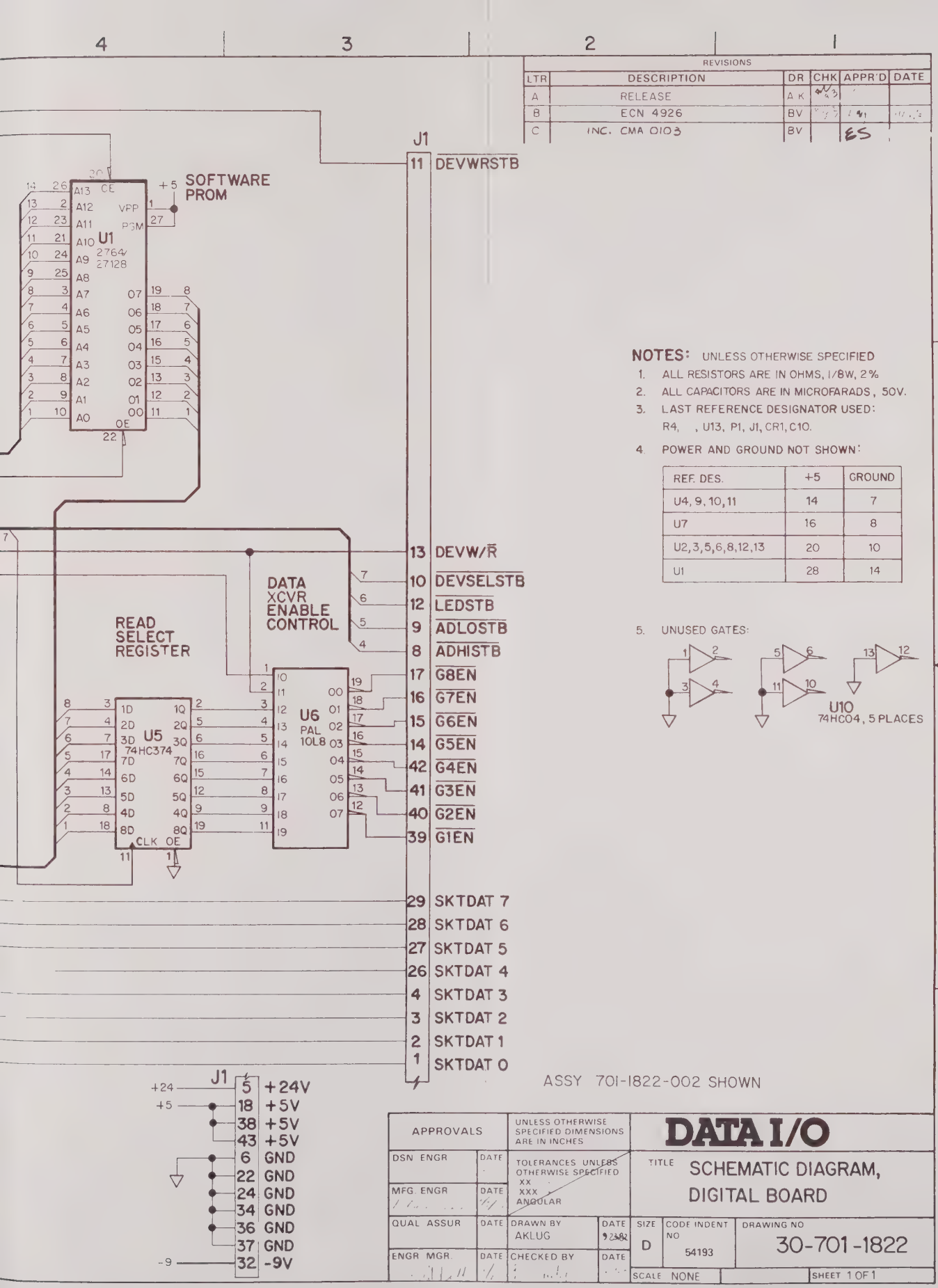
BLANK

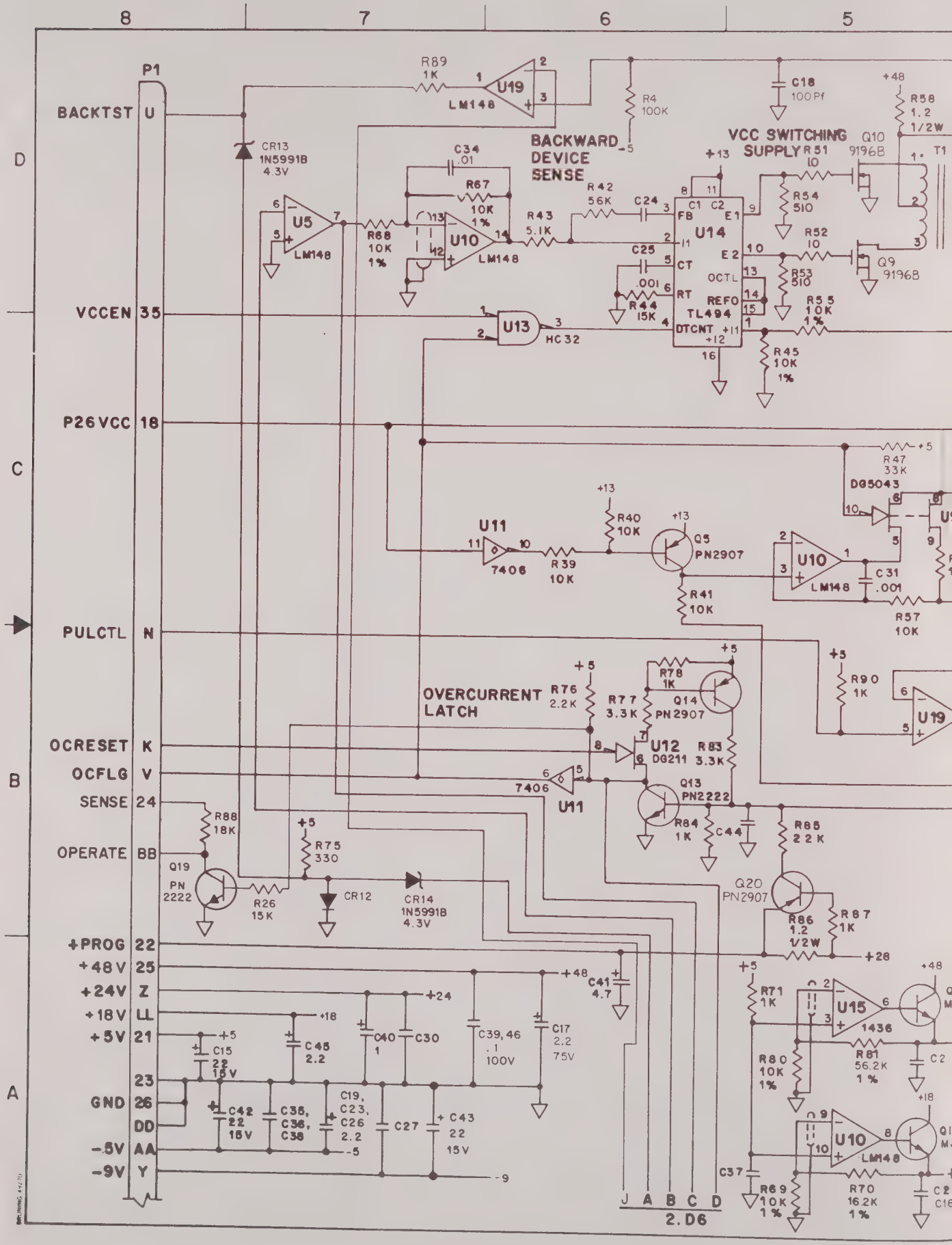
SCHEMATICS

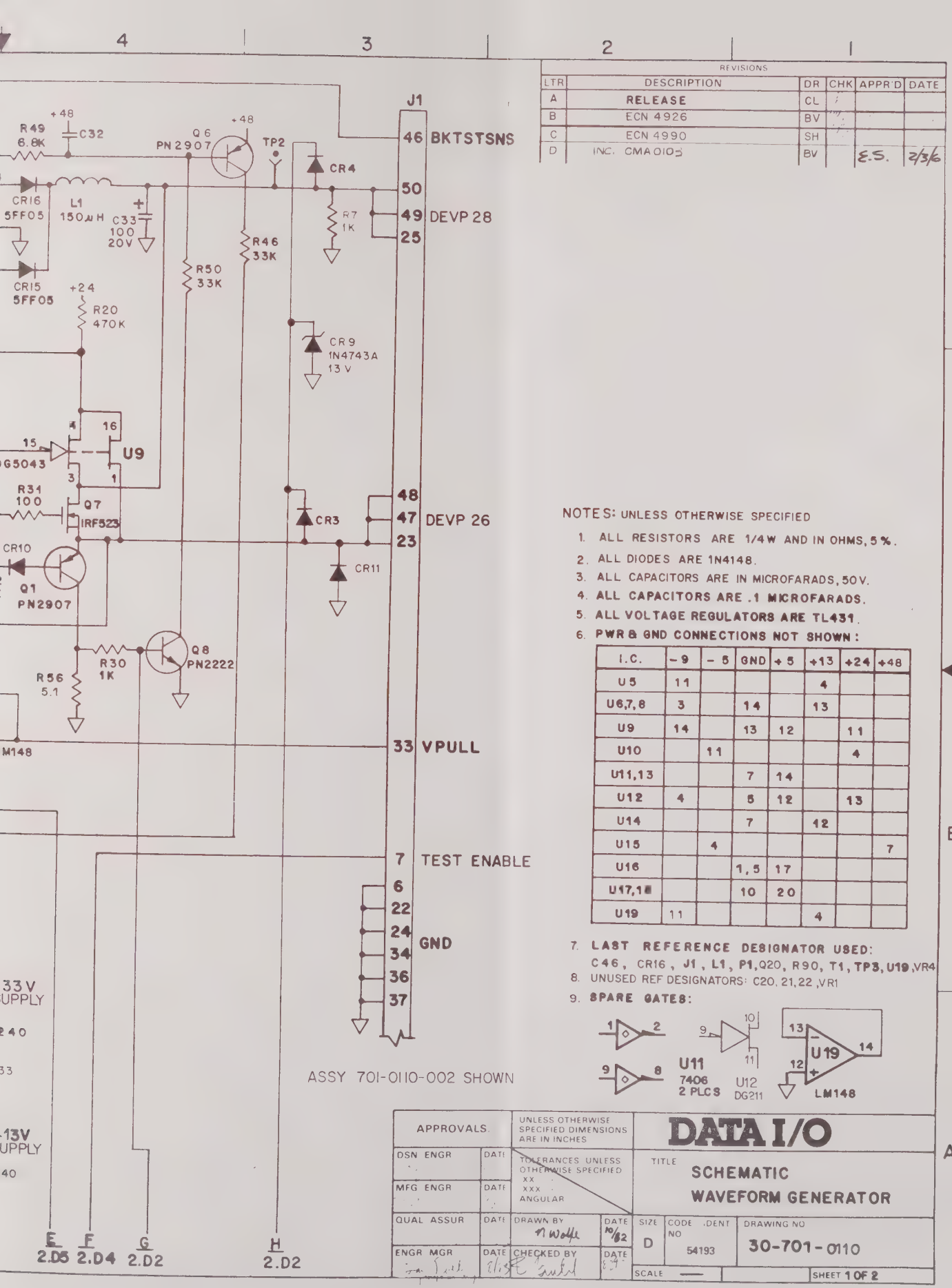
30-701-1822	Digital Card
30-701-0110	Waveform Generator
30-701-0109	Socket Board
008-1999	Motherboard

BLANK


8
7
6
5
D
C
B
A
P1
ADDRESS LATCHES
U2
74HC373
U8
74HC373
ADDRESS DECODE
U3
512 X 8
T.S.
U4
7432
4 PLACES
STROBE CONDITIONING
R2C
1K
R1E, 1K
R1B
1K
R1C, 1K
R2, 1K
R2A, 1K
R2B, 1K
R1D, 1K
U9
7409
3 PLACES
DIRECT PAGE DECODE
U10
74HC04
U7
74HC138
DIRECT PAGE ENABLES
R1A
1K
U9
7409
U11
74HC00
4 PLACES
R/W TRANSPARENT LATCH
R1F, 1K
R3, 1K
1/4W, 5%
C3, 100pF, 100V
R4
3.3K
U13
74SC245
U12
74SC245
CR1, 1N4148
C1
10
20V
C2
.1
C4,5,6,7,8,9,10
.01
A15 J
A14 8
A13 H
A12 7
A11 F
A10 6
A9 E
A8 D
A7 C
A6 B
A5 A
A4 5
A3 4
A2 3
A1 2
A0 1
A0L 27
V·Φ2 32
R/W 31
SPARE 28
PINCNTL STB HH
PINVOLT STB FF
QUALDAC STB EE
DEVW/R L
D08 16
D07 15
D06 14
D05 13
D04 12
D03 11
D02 10
D01 9
GATE ENABLE JJ
+24V Z
+5V 21
GND DD
GND 23
GND 26
-9V Y
+5
+24
-9


4
3
2
1
REVISIONS
LTR | DESCRIPTION | DR | CHK | APPR'D | DATE
A | RELEASE | A K
B | ECN 4926 | BV
C | INC. CMA 0103 | BV | ES
J1
11 DEVWRSTB
SOFTWARE PROM
+5
U1 2764/27128
13 DEVW/R
10 DEVSELSTB
12 LEDSTB
9 ADLOSTB
8 ADHISTB
17 G8EN
16 G7EN
15 G6EN
14 G5EN
42 G4EN
41 G3EN
40 G2EN
39 G1EN
DATA XCVR ENABLE CONTROL
READ SELECT REGISTER
U5 74HC374
U6 PAL 10L8
29 SKTDAT 7
28 SKTDAT 6
27 SKTDAT 5
26 SKTDAT 4
4 SKTDAT 3
3 SKTDAT 2
2 SKTDAT 1
1 SKTDAT 0
J1
+24
+5
5 +24V
18 +5V
38 +5V
43 +5V
6 GND
22 GND
24 GND
34 GND
36 GND
37 GND
-9
32 -9V
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/8W, 2%
2. ALL CAPACITORS ARE IN MICROFARADS, 50V.
3. LAST REFERENCE DESIGNATOR USED: R4, , U13, P1, J1, CR1, C10.
4. POWER AND GROUND NOT SHOWN:
REF. DES. | +5 | GROUND
U4, 9, 10, 11 | 14 | 7
U7 | 16 | 8
U2, 3, 5, 6, 8, 12, 13 | 20 | 10
U1 | 28 | 14
5. UNUSED GATES:
U10 74HC04, 5 PLACES
ASSY 701-1822-002 SHOWN
APPROVALS
DSN ENGR
MFG. ENGR
QUAL ASSUR
ENGR MGR.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED XX XXX ANGULAR
DRAWN BY AKLUG
CHECKED BY
DATA I/O
TITLE SCHEMATIC DIAGRAM, DIGITAL BOARD
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-1822
SCALE NONE
SHEET 1 OF 1


8
7
6
5
D
C
B
A
P1
BACKTST U
VCCEN 35
P26VCC 18
PULCTL N
OCRESET K
OCFLG V
SENSE 24
OPERATE BB
+PROG 22
+48V 25
+24V Z
+18V LL
+5V 21
23
GND 26
DD
-5V AA
-9V Y
R89 1K
U19 LM148
R4 100K
C18 100Pf
+48
R58 1.2 1/2W
BACKWARD DEVICE SENSE
VCC SWITCHING SUPPLY
Q10 91968
T1
CR13 1N5991B 4.3V
C34 .01
R67 10K 1%
U5 LM148
U10 LM148
R68 10K 1%
R43 5.1K
R42 56K
C24
U14
FB
E1
E2
CT
RT
REFO
OCTL
DTCNT
TL494
R54 510
R52 10
R53 510
Q9 91968
C25 .001
R44 15K
R55 10K 1%
U13 HC32
R45 10K 1%
+5
R47 33K
DG5043
U11 7406
R40 10K
Q5 PN2907
R39 10K
R41 10K
C31 .001
R57 10K
R90 1K
OVERCURRENT LATCH
R76 2.2K
R77 3.3K
R78 1K
Q14 PN2907
U12 DG211
R83 3.3K
Q13 PN2222
R84 1K
C44
R85 22K
Q20 PN2907
R86 1.2 1/2W
R87 1K
+28
R88 18K
Q19 PN 2222
R26 15K
R75 330
CR12
CR14 1N5991B 4.3V
C41 4.7
C15 22 15V
C45 2.2
C40 1
C30
C39, 46 .1 100V
C17 2.2 75V
C42 22 15V
C35, C36, C38
C19, C23, C26 2.2
C27
C43 22 15V
-5
-9
R71 1K
U15 1436
R81 56.2K 1%
R80 10K 1%
U10 LM148
C37
R69 10K 1%
R70 16.2K 1%
J A B C D
2.D6



ASSY 701-0110-002 SHOWN

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	CL			
B	ECN 4926	BV			
C	ECN 4990	SH			
D	INC. CMA0105	BV		E.S.	2/3/6

NOTES: UNLESS OTHERWISE SPECIFIED

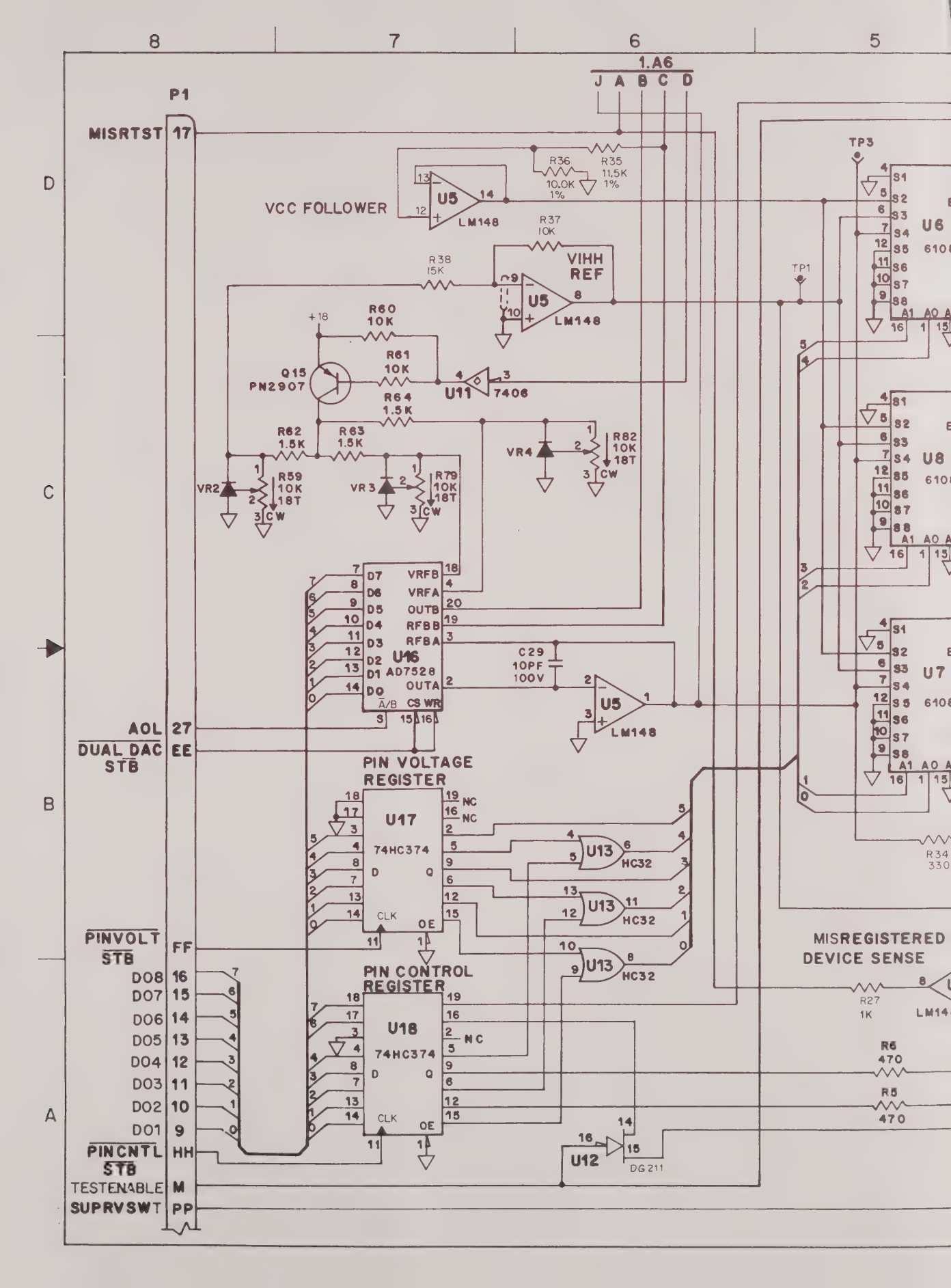
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL DIODES ARE 1N4148.
3. ALL CAPACITORS ARE IN MICROFARADS, 50V.
4. ALL CAPACITORS ARE .1 MICROFARADS.
5. ALL VOLTAGE REGULATORS ARE TL431.
6. PWR & GND CONNECTIONS NOT SHOWN:

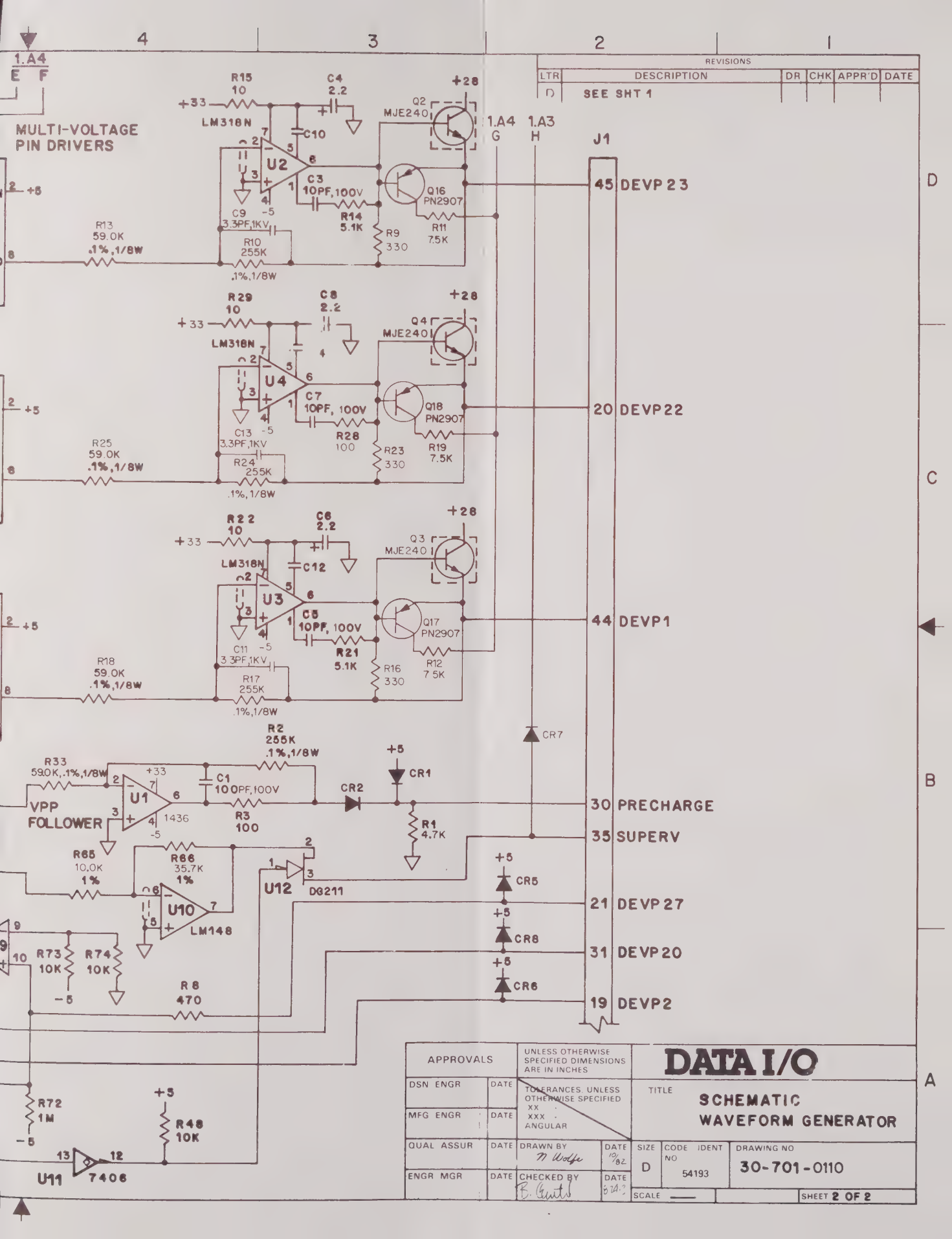
I.C.	-9	-5	GND	+5	+13	+24	+48
U5	11				4		
U6,7,8	3		14		13		
U9	14		13	12		11	
U10		11				4	
U11,13			7	14			
U12	4		5	12		13	
U14			7		12		
U15		4					7
U16			1,5	17			
U17,18			10	20			
U19	11				4		

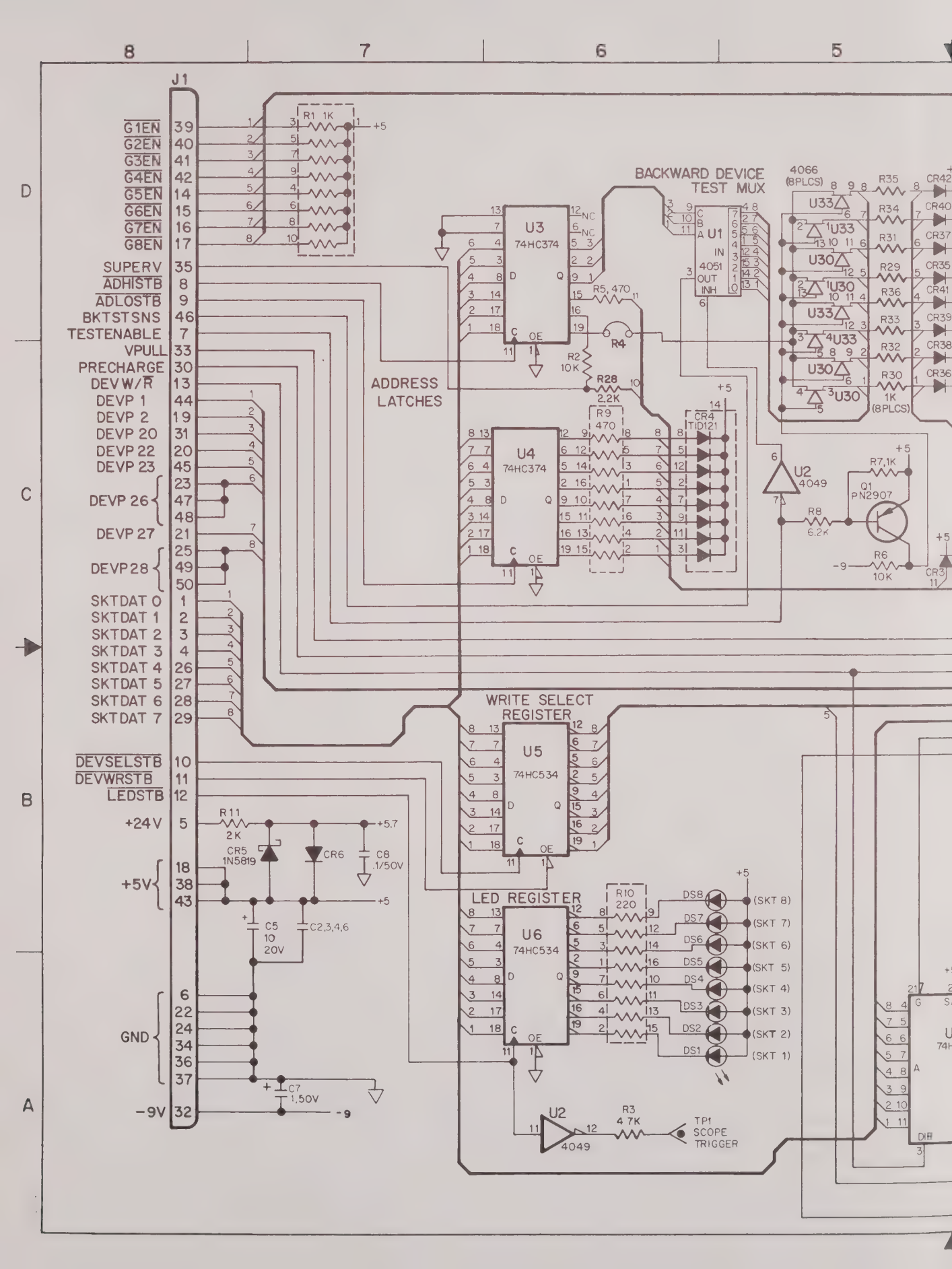
7. LAST REFERENCE DESIGNATOR USED: C46, CR16, J1, L1, P1, Q20, R90, T1, TP3, U19, VR4
8. UNUSED REF DESIGNATORS: C20, 21, 22, VR1
9. SPARE GATES:

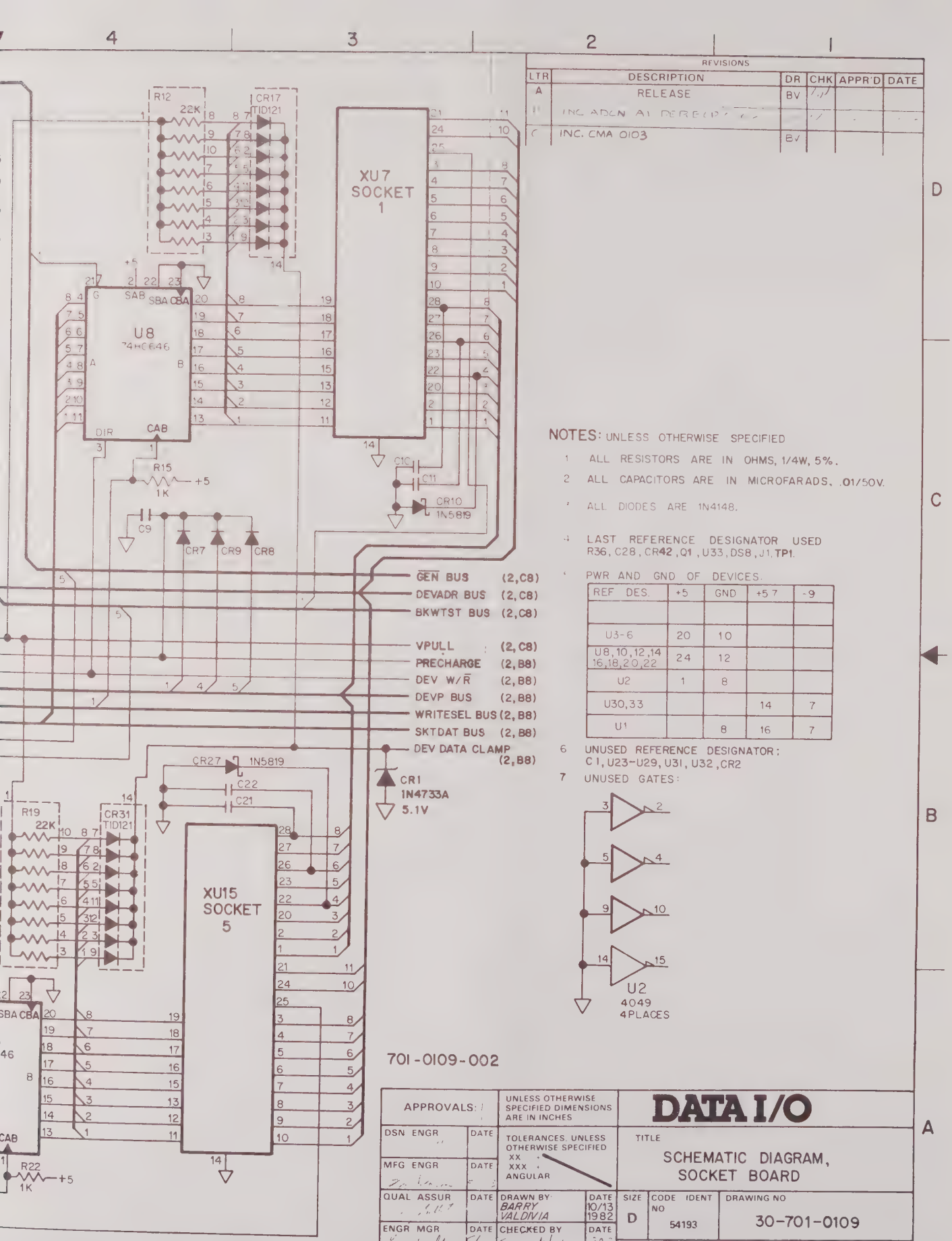
APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O		
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED XX XXX ANGULAR	TITLE SCHEMATIC WAVEFORM GENERATOR		
MFG ENGR	DATE				
QUAL ASSUR	DATE	DRAWN BY M Wolfe	DATE 10/82	SIZE D	CODE IDENT NO 54193
ENGR MGR	DATE	CHECKED BY	DATE	SCALE —	SHEET 1 OF 2

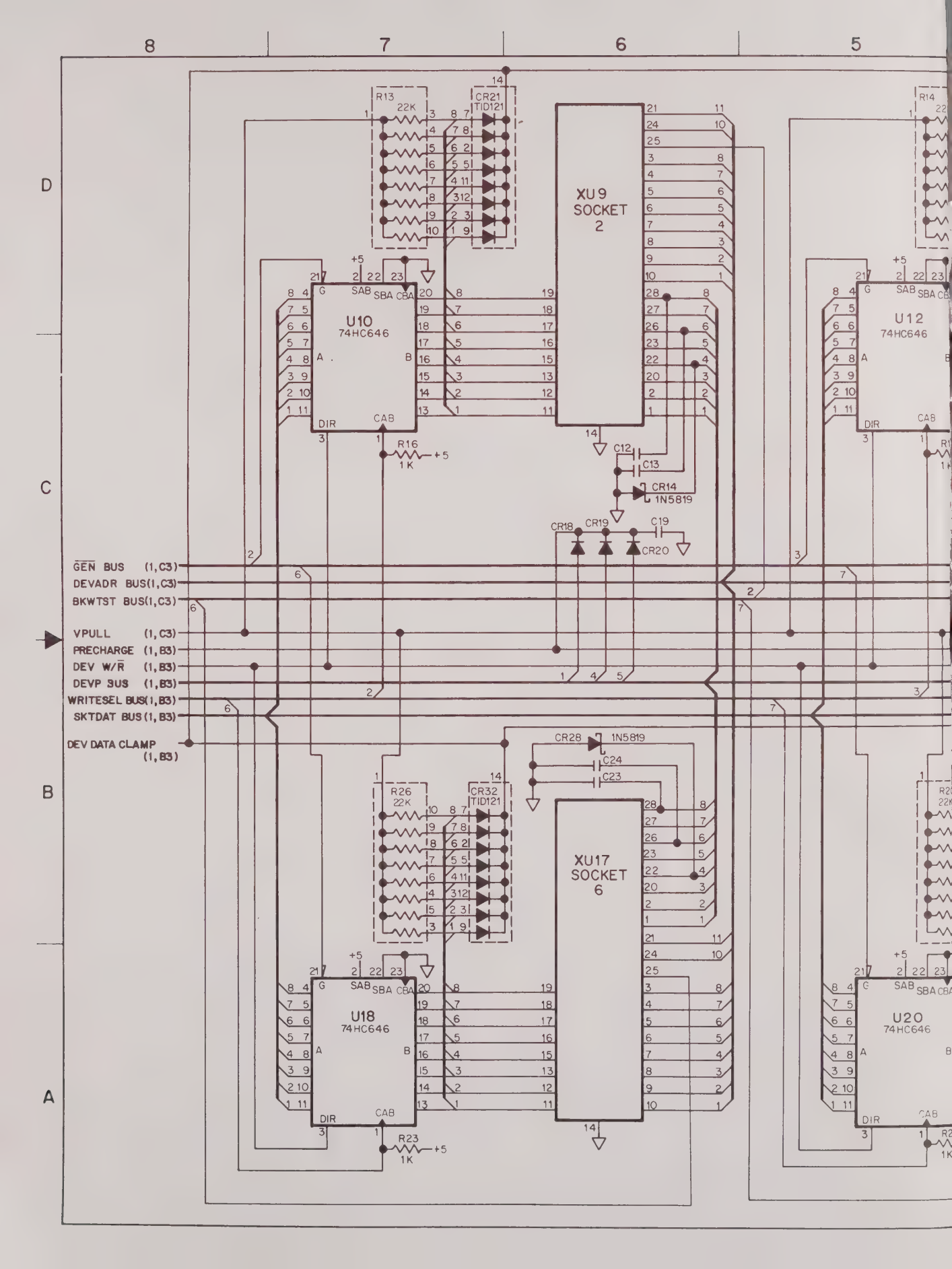
DRAWING NO 30-701-0110

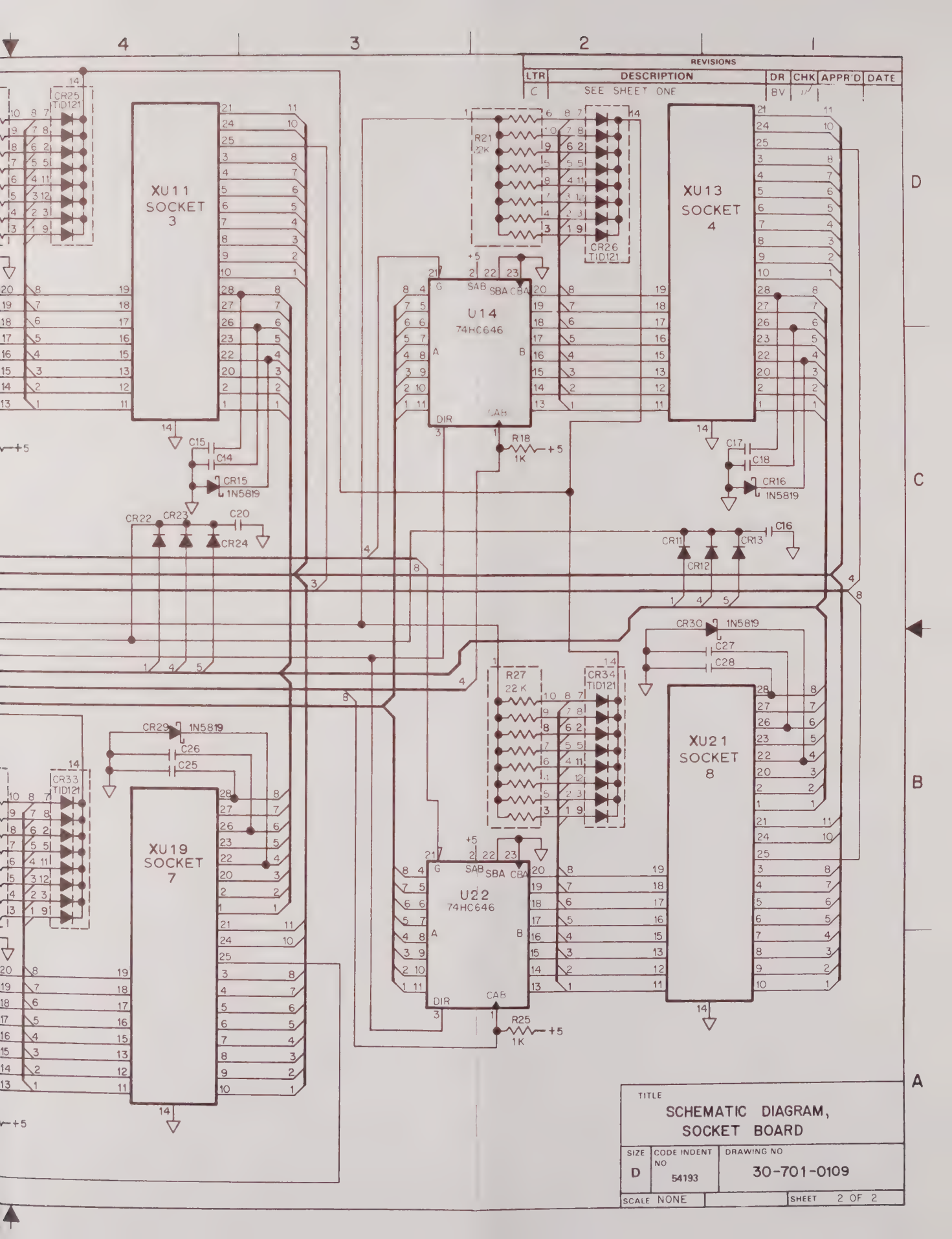

8
7
6
5
D
C
B
A
1.A6
J A B C D
P1
MISRTST 17
VCC FOLLOWER
U5
LM148
R36
10.0K
1%
R35
11.5K
1%
R37
10K
R38
15K
VIHH
REF
R60
10K
+18
Q15
PN2907
R61
10K
U11
7406
R64
1.5K
R62
1.5K
R63
1.5K
VR2
R59
10K
18T
CW
VR3
R79
10K
18T
VR4
R82
10K
18T
U16
AD7528
D7
D6
D5
D4
D3
D2
D1
D0
VRFB
VRFA
OUTB
RFBB
RFBA
OUTA
A/B
CS
WR
C29
10PF
100V
AOL 27
DUAL DAC STB EE
PIN VOLTAGE REGISTER
U17
74HC374
D
Q
CLK
OE
NC
U13
HC32
PINVOLT STB FF
PIN CONTROL REGISTER
U18
DO8 16
DO7 15
DO6 14
DO5 13
DO4 12
DO3 11
DO2 10
DO1 9
PINCNTL STB HH
TESTENABLE M
SUPRVSWT PP
U12
DG211
TP3
TP1
U6
U8
U7
A1 A0
R34
330
MISREGISTERED
DEVICE SENSE
R27
1K
R6
470
R5
470

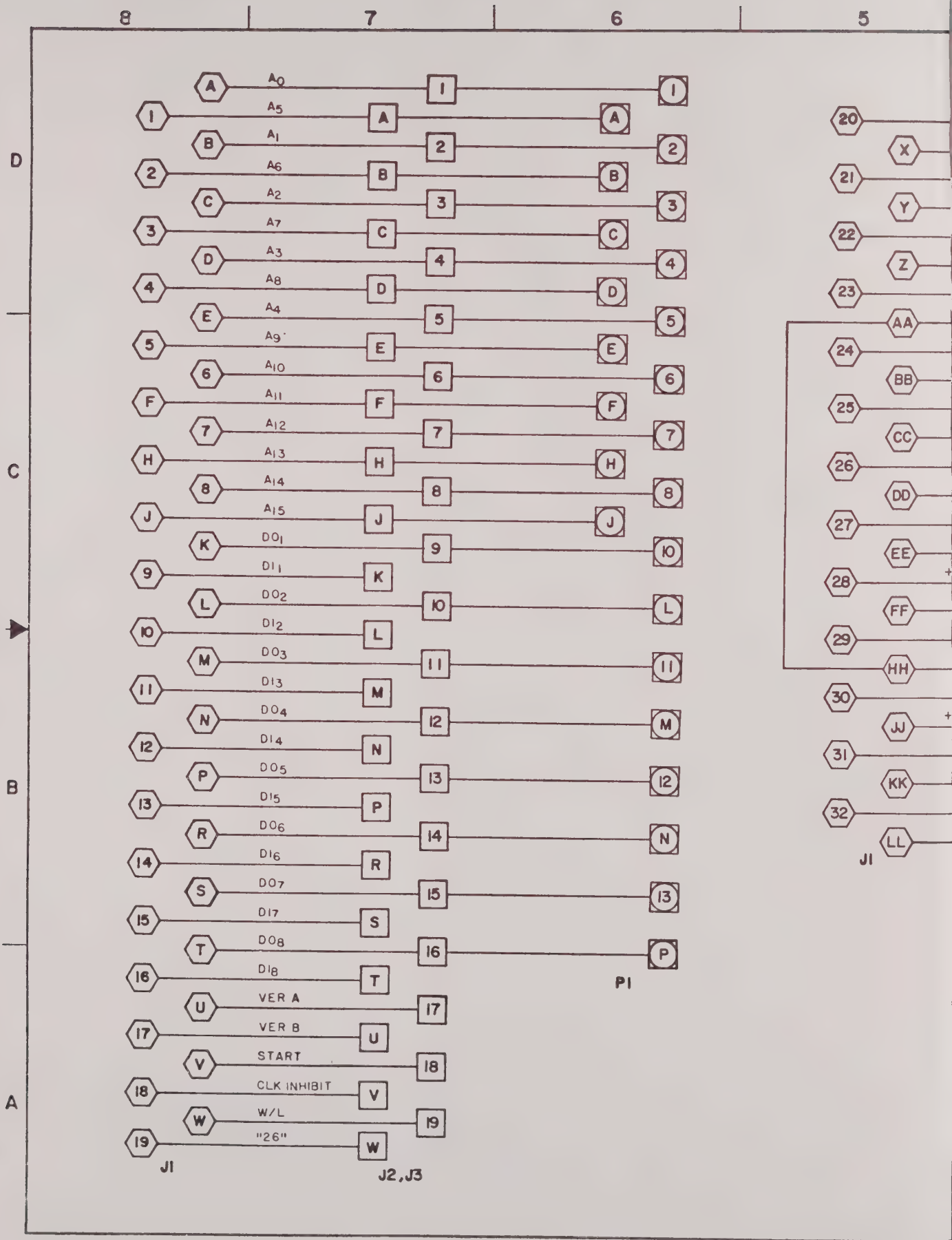

4
3
2
1
REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
D SEE SHT 1
1.A4 E F
MULTI-VOLTAGE PIN DRIVERS
R15 10
C4 2.2
+33
LM318N
C10
U2
Q2 MJE240
+28
C3 10PF,100V
R14 5.1K
Q16 PN2907
R11 7.5K
R9 330
C9 3.3PF,1KV
R10 255K .1%,1/8W
R13 59.0K .1%,1/8W
1.A4 G
1.A3 H
J1
45 DEVP23
R29 10
C8 2.2
U4
Q4 MJE240
C7 10PF, 100V
R28 100
Q18 PN2907
R19 7.5K
R23 330
C13 3.3PF,1KV
R24 255K .1%,1/8W
R25 59.0K .1%,1/8W
20 DEVP22
R22 10
C6 2.2
U3
Q3 MJE240
C12
C5 10PF, 100V
R21 5.1K
Q17 PN2907
R12 7.5K
R16 330
C11 3.3PF,1KV
R17 255K .1%,1/8W
R18 59.0K .1%,1/8W
44 DEVP1
CR7
R2 255K .1%,1/8W
R33 59.0K,.1%,1/8W
VPP FOLLOWER
U1
1436
C1 100PF,100V
R3 100
CR2
CR1
+5
R1 4.7K
30 PRECHARGE
35 SUPERV
R65 10.0K 1%
R66 35.7K 1%
U10 LM148
U12 DG211
CR5
21 DEVP27
CR8
31 DEVP20
CR6
19 DEVP2
R73 10K
R74 10K
R8 470
R72 1M
R48 10K
U11 7406
APPROVALS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DSN ENGR DATE
MFG ENGR DATE
QUAL ASSUR DATE
ENGR MGR DATE
TOLERANCES UNLESS OTHERWISE SPECIFIED
XX .
XXX .
ANGULAR
DRAWN BY M Wolfe DATE 1/82
CHECKED BY B. Curtis DATE 3-24-82
DATA I/O
TITLE
SCHEMATIC
WAVEFORM GENERATOR
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-0110
SCALE
SHEET 2 OF 2

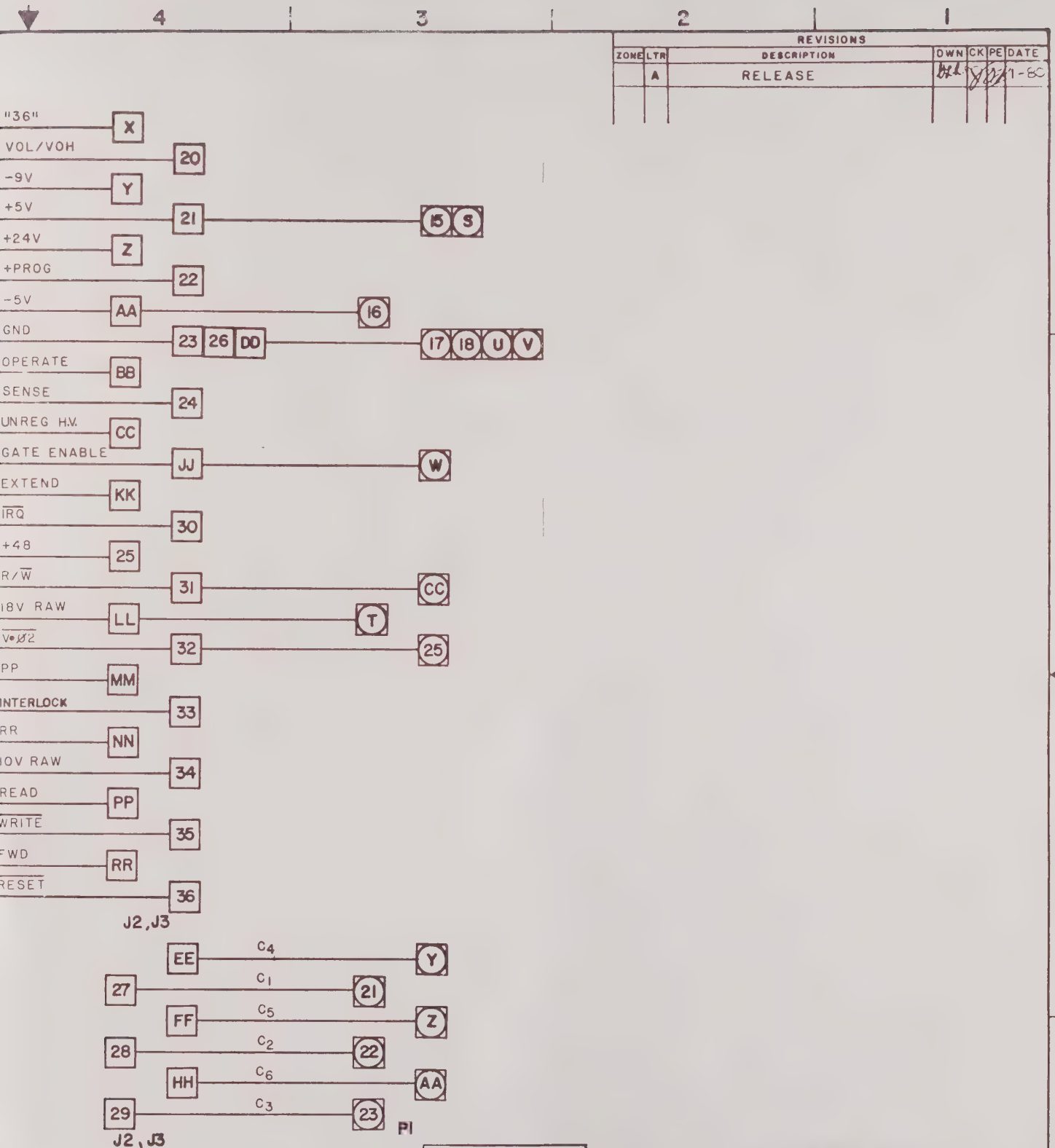

8
7
6
5
D
C
B
A
J1
G1EN 39
G2EN 40
G3EN 41
G4EN 42
G5EN 14
G6EN 15
G7EN 16
G8EN 17
SUPERV 35
ADHISTB 8
ADLOSTB 9
BKTSTSNS 46
TESTENABLE 7
VPULL 33
PRECHARGE 30
DEVW/R 13
DEVP 1 44
DEVP 2 19
DEVP 20 31
DEVP 22 20
DEVP 23 45
DEVP 26 23 47 48
DEVP 27 21
DEVP 28 25 49 50
SKTDAT 0 1
SKTDAT 1 2
SKTDAT 2 3
SKTDAT 3 4
SKTDAT 4 26
SKTDAT 5 27
SKTDAT 6 28
SKTDAT 7 29
DEVSELSTB 10
DEVWRSTB 11
LEDSTB 12
+24V 5
+5V 18 38 43
GND 6 22 24 34 36 37
-9V 32
R1 1K
+5
ADDRESS LATCHES
U3
74HC374
R5, 470
R4
R2 10K
R28 2.2K
U4
74HC374
R9 470
CR4 TID121
BACKWARD DEVICE TEST MUX
U1
4051
IN
OUT
INH
4066 (8PLCS)
U33
U30
R35
R34
R31
R29
R36
R33
R32
R30 1K (8PLCS)
CR42
CR40
CR37
CR35
CR41
CR39
CR38
CR36
U2
4049
R7,1K
Q1 PN2907
R8 6.2K
R6 10K
CR3
WRITE SELECT REGISTER
U5
74HC534
LED REGISTER
U6
74HC534
R10 220
DS8
DS7
DS6
DS5
DS4
DS3
DS2
DS1
(SKT 8)
(SKT 7)
(SKT 6)
(SKT 5)
(SKT 4)
(SKT 3)
(SKT 2)
(SKT 1)
R11 2K
CR5 1N5819
CR6
C8 .1/50V
+5.7
C5 10 20V
C2,3,4,6
C7 1,50V
-9
U2
4049
R3 4.7K
TP1 SCOPE TRIGGER


4
3
2
1
D
C
B
A
REVISIONS
LTR | DESCRIPTION | DR | CHK | APPR'D | DATE
A | RELEASE | BV
C | INC. CMA 0103 | BV
R12
22K
CR17
TID121
XU7
SOCKET
1
U8
74HC646
SAB
SBA
CBA
DIR
CAB
R15
1K
+5
C9
CR7
CR9
CR8
C10
C11
CR10
1N5819
GEN BUS (2,C8)
DEVADR BUS (2,C8)
BKWTST BUS (2,C8)
VPULL (2,C8)
PRECHARGE (2,B8)
DEV W/R̄ (2,B8)
DEVP BUS (2,B8)
WRITESEL BUS (2,B8)
SKTDAT BUS (2,B8)
DEV DATA CLAMP (2,B8)
CR1
1N4733A
5.1V
CR27
1N5819
C22
C21
R19
22K
CR31
TID121
XU15
SOCKET
5
R22
1K
+5
NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2 ALL CAPACITORS ARE IN MICROFARADS, .01/50V.
3 ALL DIODES ARE 1N4148.
4 LAST REFERENCE DESIGNATOR USED R36, C28, CR42, Q1, U33, DS8, J1, TP1.
5 PWR AND GND OF DEVICES.
REF DES. | +5 | GND | +5 7 | -9
U3-6 | 20 | 10
U8,10,12,14 16,18,20,22 | 24 | 12
U2 | 1 | 8
U30,33 | | | 14 | 7
U1 | | 8 | 16 | 7
6 UNUSED REFERENCE DESIGNATOR: C1, U23-U29, U31, U32, CR2
7 UNUSED GATES:
U2
4049
4PLACES
701-0109-002
APPROVALS:
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES, UNLESS OTHERWISE SPECIFIED
XX
XXX
ANGULAR
DSN ENGR | DATE
MFG ENGR | DATE
QUAL ASSUR | DATE
ENGR MGR | DATE
DRAWN BY: BARRY VALDIVIA | DATE 10/13 1982
CHECKED BY | DATE
DATA I/O
TITLE
SCHEMATIC DIAGRAM, SOCKET BOARD
SIZE D
CODE IDENT NO 54193
DRAWING NO 30-701-0109
SCALE NONE
SHEET 1 OF 2


8
7
6
5
D
C
B
A
R13
22K
CR21
TID121
XU9
SOCKET
2
U10
74HC646
R16
1K
+5
C12
C13
CR14
1N5819
CR18
CR19
C19
CR20
U12
74HC646
GEN BUS (1,C3)
DEVADR BUS(1,C3)
BKWTST BUS(1,C3)
VPULL (1,C3)
PRECHARGE (1,B3)
DEV W/R (1,B3)
DEVP BUS (1,B3)
WRITESEL BUS(1,B3)
SKTDAT BUS(1,B3)
DEV DATA CLAMP (1,B3)
CR28
1N5819
C24
C23
R26
22K
CR32
TID121
XU17
SOCKET
6
U18
74HC646
R23
1K
U20
74HC646


4
3
2
1
REVISIONS
LTR
DESCRIPTION
DR
CHK
APPR'D
DATE
C
SEE SHEET ONE
BV
D
C
B
A
XU11 SOCKET 3
XU13 SOCKET 4
XU19 SOCKET 7
XU21 SOCKET 8
U14 74HC646
U22 74HC646
R21 22K
R27 22K
R18 1K
R25 1K
CR25 TID121
CR26 TID121
CR33 TID121
CR34 TID121
CR15 1N5819
CR16 1N5819
CR29 1N5819
CR30 1N5819
CR11
CR12
CR13
CR22
CR23
CR24
C14
C15
C16
C17
C18
C20
C25
C26
C27
C28
+5
SAB
SBA
CBA
CAB
DIR
TITLE
SCHEMATIC DIAGRAM, SOCKET BOARD
SIZE
D
CODE INDENT NO
54193
DRAWING NO
30-701-0109
SCALE NONE
SHEET 2 OF 2


8
7
6
5
D
C
B
A
A0
A5
A1
A6
A2
A7
A3
A8
A4
A9
A10
A11
A12
A13
A14
A15
DO1
DI1
DO2
DI2
DO3
DI3
DO4
DI4
DO5
DI5
DO6
DI6
DO7
DI7
DO8
DI8
VER A
VER B
START
CLK INHIBIT
W/L
"26"
J1
J2,J3
P1
J1



APPROVALS	TOLERANCES (EXCEPT AS NOTED)	DATA I/O
PROJ. ENG.	DECIMAL ±	TITLE SCHEMATIC DIAGRAM UniPak MOTHERBOARD
PROD. ENG.	ANGULAR ±	
CONF. MANG.	DRAWN BY G RYDER	SIZE D · CODE IDENT NO · DRAWING NO 008-1999
ENG. MGR.	CHECK	SCALE NA · SHEET 1 OF 1
DATE 1-17-80		

U.S. Sales Offices and Representatives
Direct Sales and Service Offices

Data I/O Corporation
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
Telex Dom. 15-2167,
Int'l. 4740166 DIO UI

NORTHWEST REGION

Data I/O Corporation
1700 Wyatt Drive
Suite 1
Santa Clara, CA 95054
(408) 727-0641

SOUTHWEST REGION

Data I/O Corporation
2770 South Harbor Blvd.
Suite K
Santa Ana, CA 92704
(714) 662-1182 *(Sales)*
(714) 662-2498 *(Service)*
Telex 755870

EASTERN REGION

Data I/O Corporation
Nashua Road
Route 101A
Amherst, NH 03031
(603) 889-8511 *(Sales)*
(603) 889-8513 *(Service)*
Telex 943431

CENTRAL REGION

Data I/O Corporation
1810 N. Glenville Drive
Suite 108
Richardson, TX 75081
(214) 235-0044
Telex 792474

Representatives

ALASKA, WASHINGTON (TRI-CITIES, VANCOUVER), OREGON

Northwest Test and Measurement
8196 Southwest Hall
Suite 217
Beaverton, OR 97005
(503) 646-9966
1-800-247-5700
Telex 910-467-8775

WESTERN WASHINGTON, SPOKANE

Northwest Test and Measurement
4020 148th Ave. N.E.
Suite F
Redmond, WA 98052
(206) 881-8857

ARKANSAS, LOUISIANA, OKLAHOMA, TEXAS

TESTECH, Inc.
1000 E. Campbell Road
Suite 108
Richardson, TX 75081
(214) 644-5010

4800 West 34th St.
Suite D-6
Houston, TX 77092
(713) 956-0837

1715 Capital of Texas Hwy S.
Suite 107
Austin, TX 78746
(512) 327-7033

OHIO

Electro Sales Associates
1635 Mardon Drive
Dayton, OH 45432
(513) 426-5551

26250 Euclid Avenue
Suite 331
Cleveland, OH 44132
(216) 261-5440

MICHIGAN

Electro Sales Associates
29200 Vassar Road
Suite 505
Livonia, MI 48152
(313) 474-7320

9816 Portage Road
Portage, MI 49002
(616) 323-2416

PENNSYLVANIA, WEST VIRGINIA, EASTERN KENTUCKY

Electro Sales Associates
3740 Mount Royal Blvd.
Allison Park, PA 15101
(412) 487-3801

UPSTATE NEW YORK

DB Associates, Inc.
7000 E. Genesee Street
Building D
Fayetteville, NY 13066
(315) 446-0220

KANSAS, NEBRASKA

Midtec Associates, Inc.
7702 Mize Road
DeSoto, KS 66018
(913) 441-6565
Telex 910-743-4129

MISSOURI

Midtec Associates, Inc.
8460 Lindbergh North
Suite 11
Florissant, MO 63031
(314) 837-5200

FLORIDA

Pen Tech Associates
201 S.E. 15th Terrace
Suite K
Deerfield Beach, FL 33441
(305) 421-4989

1398 Semoran Blvd.
Suite 106
Casselberry, FL 32707
(305) 645-3444

GEORGIA, TENNESSEE

Pen Tech Associates
627 Cherokee Street
Suite 21
Marietta, GA 30060
(404) 424-1931

NORTHERN FLORIDA, ALABAMA, TENNESSEE, MISSISSIPPI

Pen Tech Associates
3322 Memorial Pkwy. S.W.
Suite 36
Huntsville, AL 35801
(205) 881-9298

NORTH CAROLINA, SOUTH CAROLINA

Pen Tech Associates
3709 Alliance Drive
Suite C
Greensboro, NC 27407
(919) 852-6000

MINNESOTA, NORTH DAKOTA, SOUTH DAKOTA

Torkelson Associates
4940 Viking Drive
Minneapolis, MN 55435
(612) 835-2414
Telex 910-576-2740

NORTHERN ILLINOIS, IOWA, INDIANA

Torkelson Associates
108 Wilmot Road, Suite 110
Deerfield, IL 60015
(312) 945-8700
Telex 910-992-1438

INDIANA, WESTERN KENTUCKY

Torkelson Associates
2346 S. Lynhurst
Room B101
Indianapolis, IN 46241
(317) 244-7867
Telex 810-341-3141

WISCONSIN

Torkelson Associates
2840 N. Brookfield Road
Brookfield, WI 53005
(414) 784-7736

ARIZONA, NEVADA

Zeus Electronics, Inc.
1428 E. Pierson Street
Phoenix, AZ 85014
(602) 263-6022
1-800-528-4512
Telex 910-951-1362

NEW MEXICO, EL PASO CO., TEXAS

Zeus Electronics, Inc.
8100 Mountain Road N.E.
Suite 111
Albuquerque, NM 87110
(505) 842-6633
1-800-528-4512

COLORADO, WYOMING

Zeus Electronics, Inc.
3333 Quebec Street
Suite 2950
Denver, CO 80207
(303) 321-4246
1-800-528-4512

UTAH, IDAHO, MONTANA

Zeus Electronics, Inc.
1849 W. North Temple
Suite B105
Salt Lake City, UT 84116
(801) 534-0500
(801) 534-0503

VIRGINIA, WASHINGTON D.C.

SCI-REP, Inc.
9512A Lee Highway
Fairfax, VA 22031
(703) 385-0600
Telex 710-833-0361

NEW JERSEY, EASTERN PENNSYLVANIA

SCI-REP, Inc.
304 Cooper Center
Pennsauken, NJ 08109
(609) 662-5222
Telex 710-892-1297 SCI-REP PESN

Addresses on this list subject to change without notice.

0321/784

International Sales Offices and Representatives

Europe

Data I/O Europe
Vondelstraat 50-52
NL-1054 GE Amsterdam
The Netherlands
(20)186855
Telex 16616 DATIO NL

Data I/O Germany GmbH
Bahnhofstrasse 3
D-6453 Seligenstadt
West Germany
(6182)3088/89
Telex 4184962 DATA D

AUSTRIA

Ing. Ernst Steiner
Hummelgasse 14
A-1130 Wien
Austria
(222)827474
Telex 135026 ES A

BELGIUM

Simac Electronics
Rue du Progres 52
BOITE 3
B-1000 Brussels
Belgium
(2)2192451-3
Telex 23662 SIMEIP B

DENMARK

ITT Multikomponent A/S
Naverland 29
DK-2600 Glostrup
Denmark
(2)451822 or (2)456645
Telex 33355 ITT DK

FINLAND

Instrumentarium Elektroniikka
PL 64 (Vitikka 1)
SF-02630 ESPOO 63
Finland
(358)0905281
Telex 124426 HAVUL SF

FRANCE

M.B. Electronique
606, rue Fourny
Zac de Buc
P.O. Box 31
F-78530, Buc, France
(3)9568131
Telex MB 695414 F

GERMANY

Instrumatic Electronics GmbH
Am Kirchenholzel 14
D-8032 Grafelfing (near Munich)
West Germany
(89)852063
Telex 524298 INSTR D

GREECE

Eltronics Ltd.
2, Alopekis Str. 52
GR-106 75 Athens 139
(1) 7249511/-15
Telex 216589 DARX GR

ISRAEL

TELSYS, Ltd.
12, Kehilat Venetsia Street
Tel-Aviv 69010
Israel
(3)494891-5/(3)494881-2
Telex 32392 TSEE IL

ITALY

Sistrel SPA
Via Giuseppe Armellini 39
I-00143 Roma
Italy
(6)5915551
Telex 680356 SISTREL I

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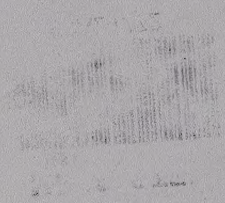

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